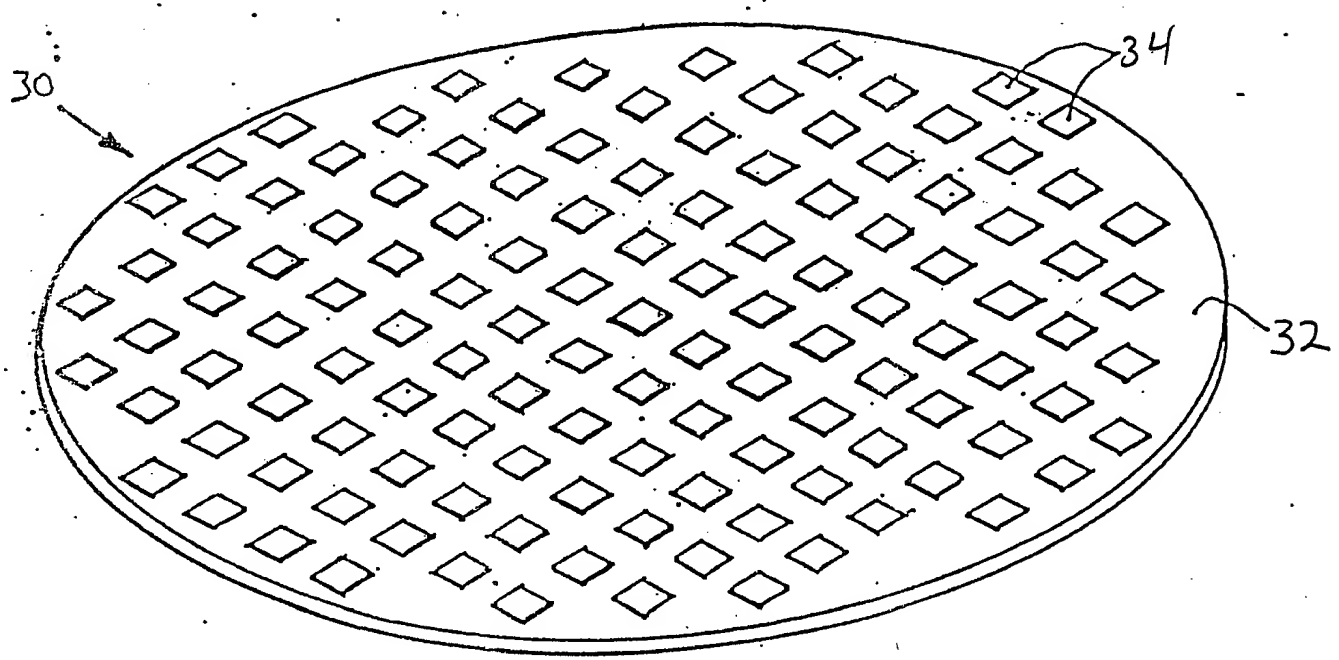


FIGURE 1

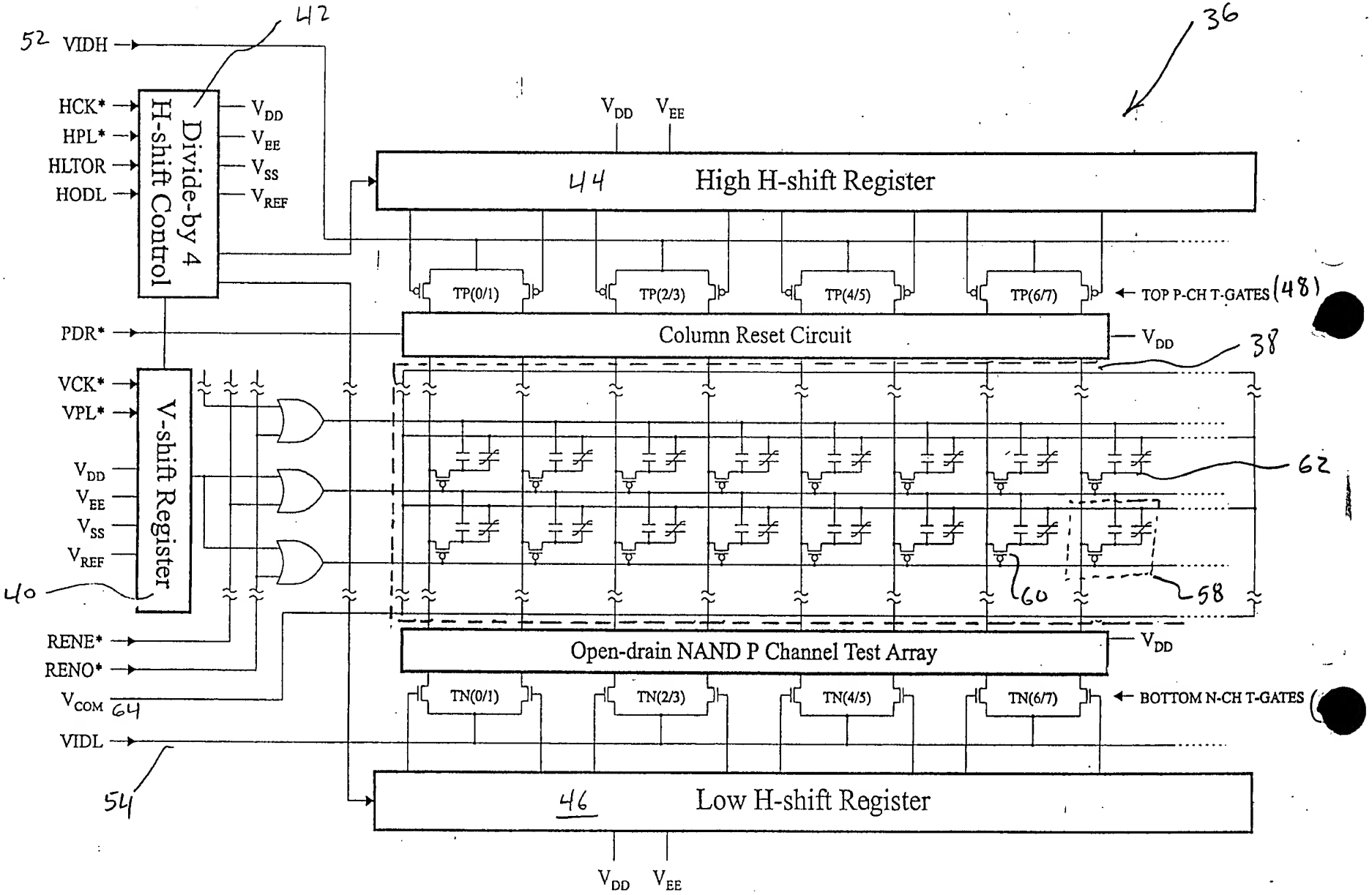


FIGURE 2A

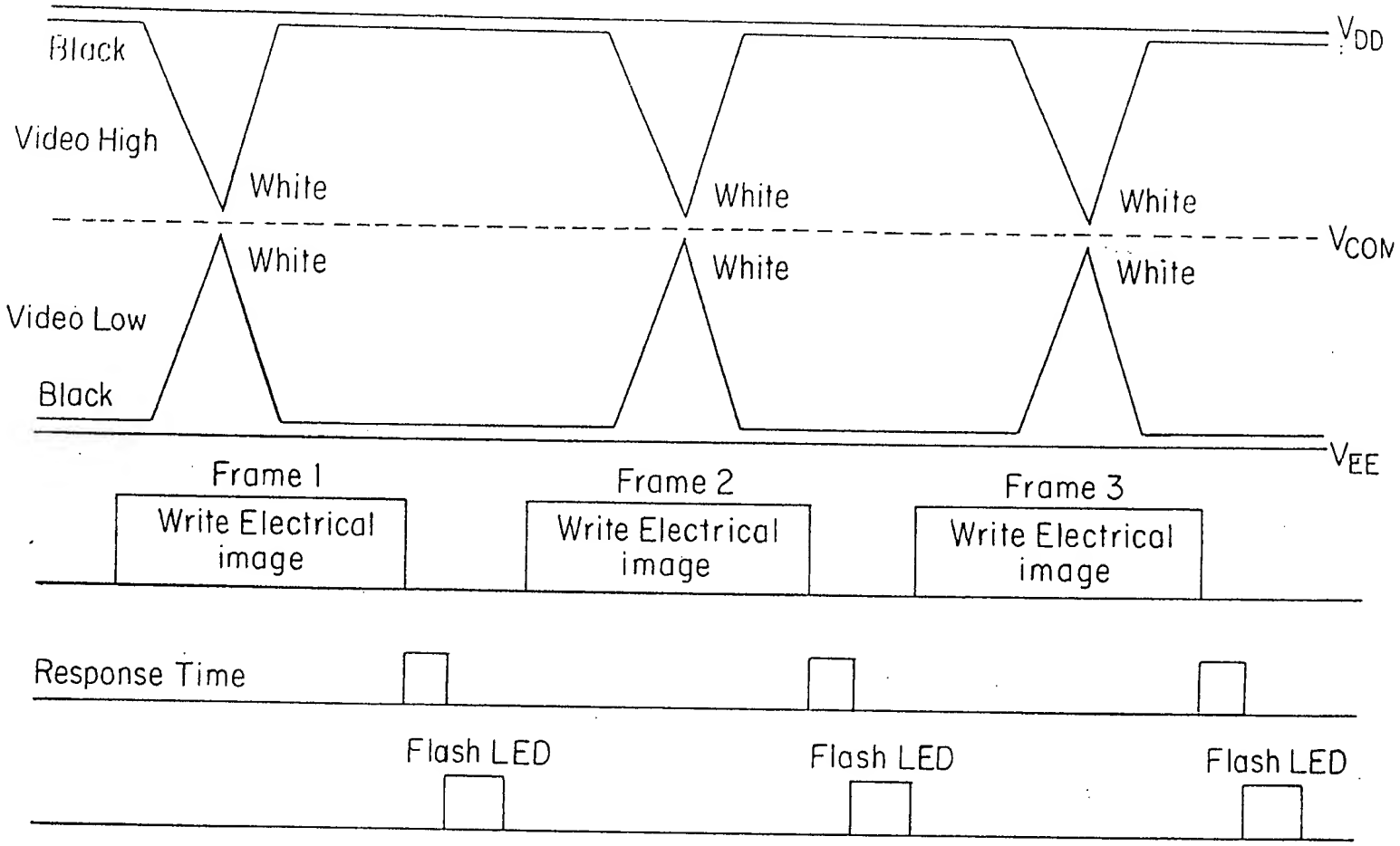

Black
Video High
White
White
White
V_{DD}
V_{COM}
White
White
White
Video Low
Black
V_{EE}
Frame 1
Write Electrical image
Frame 2
Write Electrical image
Frame 3
Write Electrical image
Response Time
Flash LED
Flash LED
Flash LED

FIGURE 2B

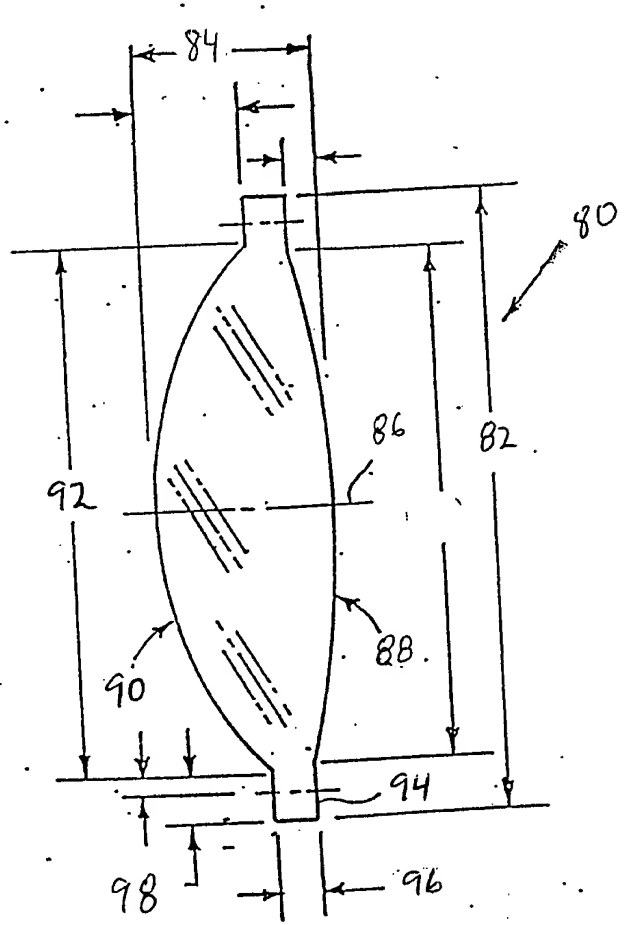


FIGURE 3A

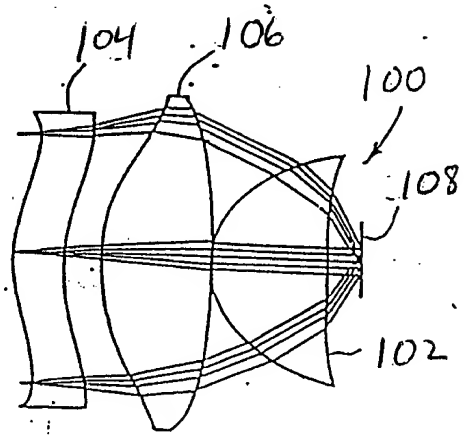


FIGURE 3B

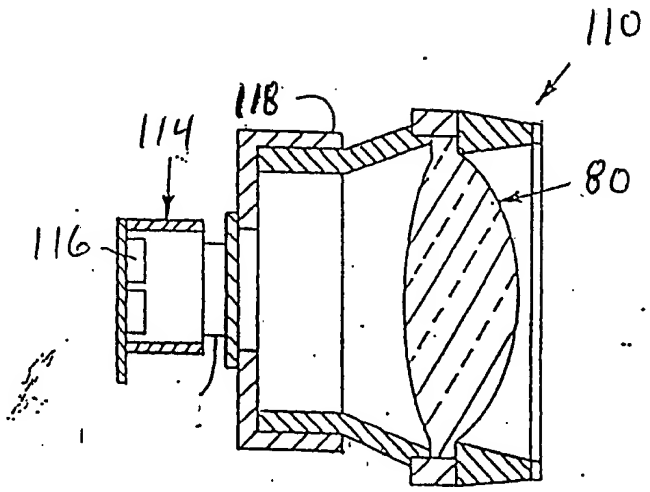


FIGURE 3C

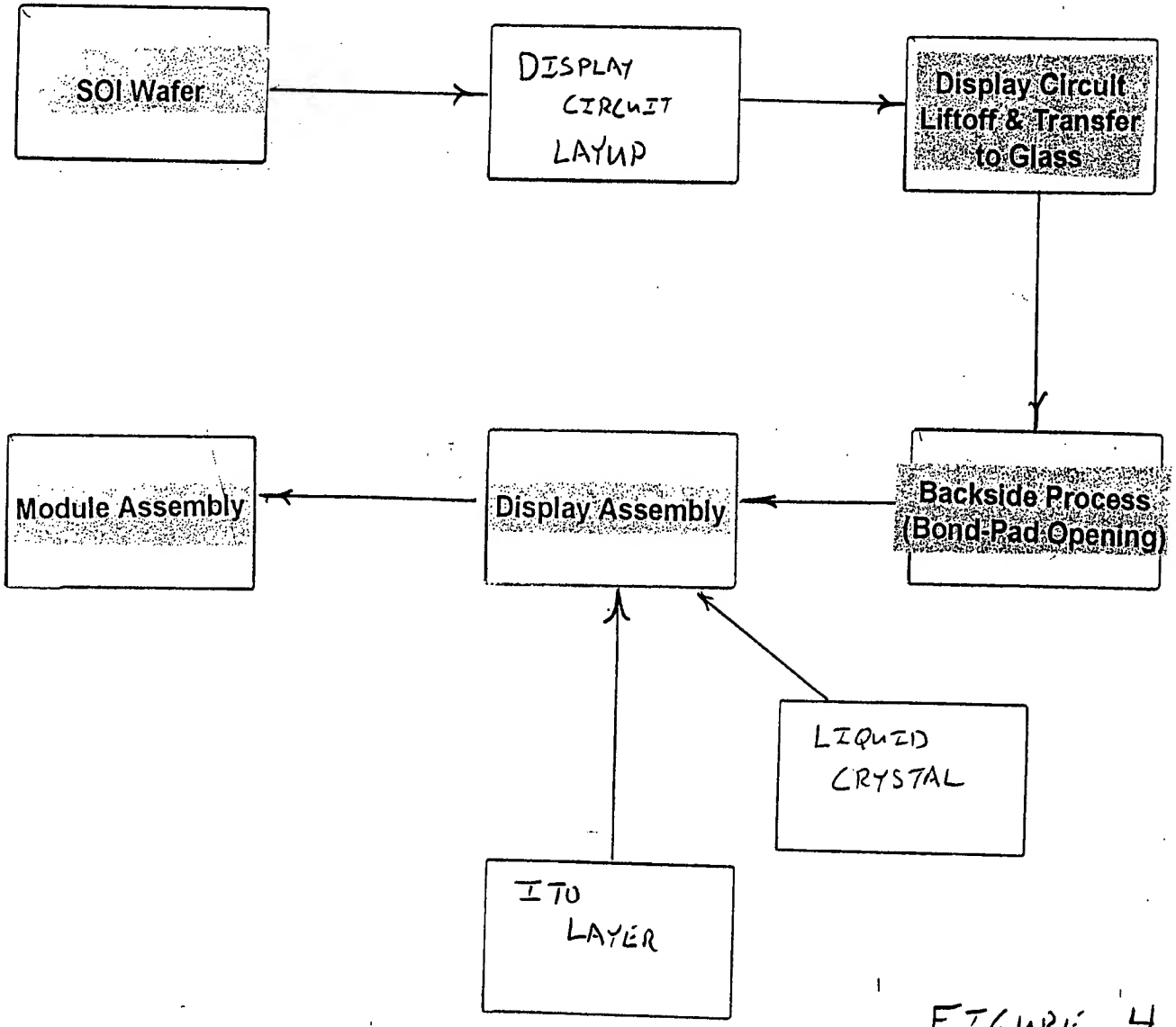


FIGURE 4

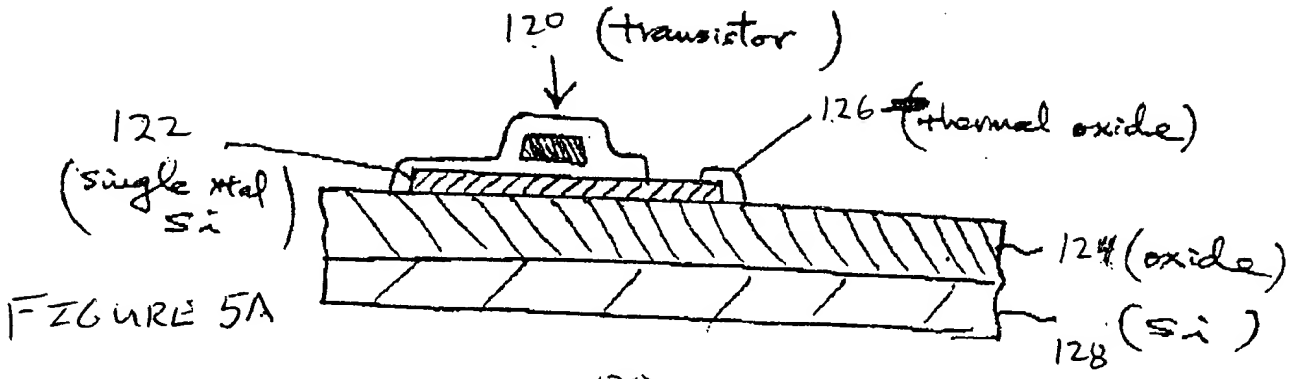


FIGURE 5A

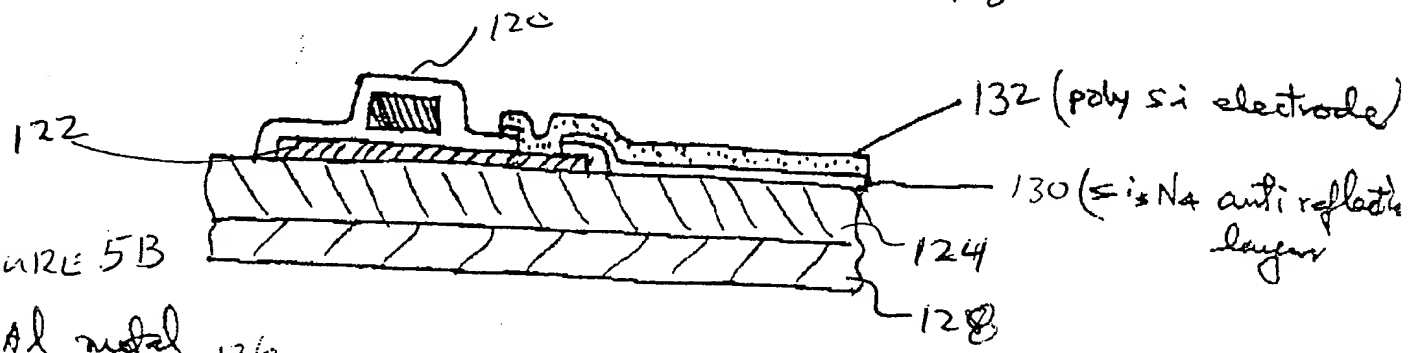


FIGURE 5B

Al metal

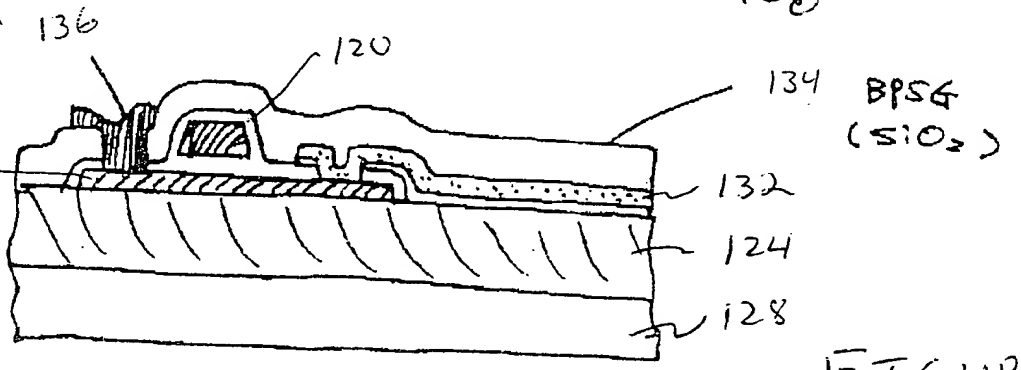


FIGURE 5C

(Si3N4 passivation)

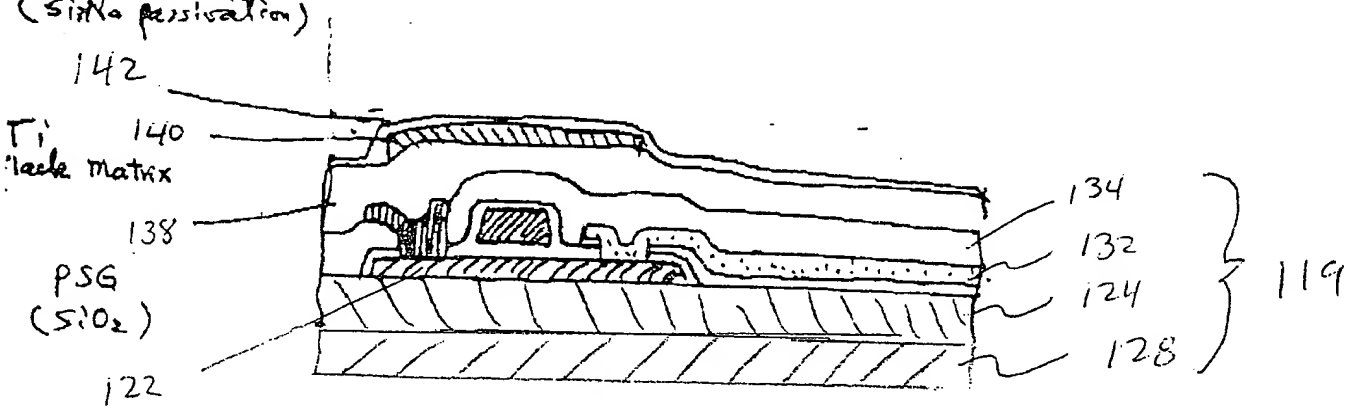
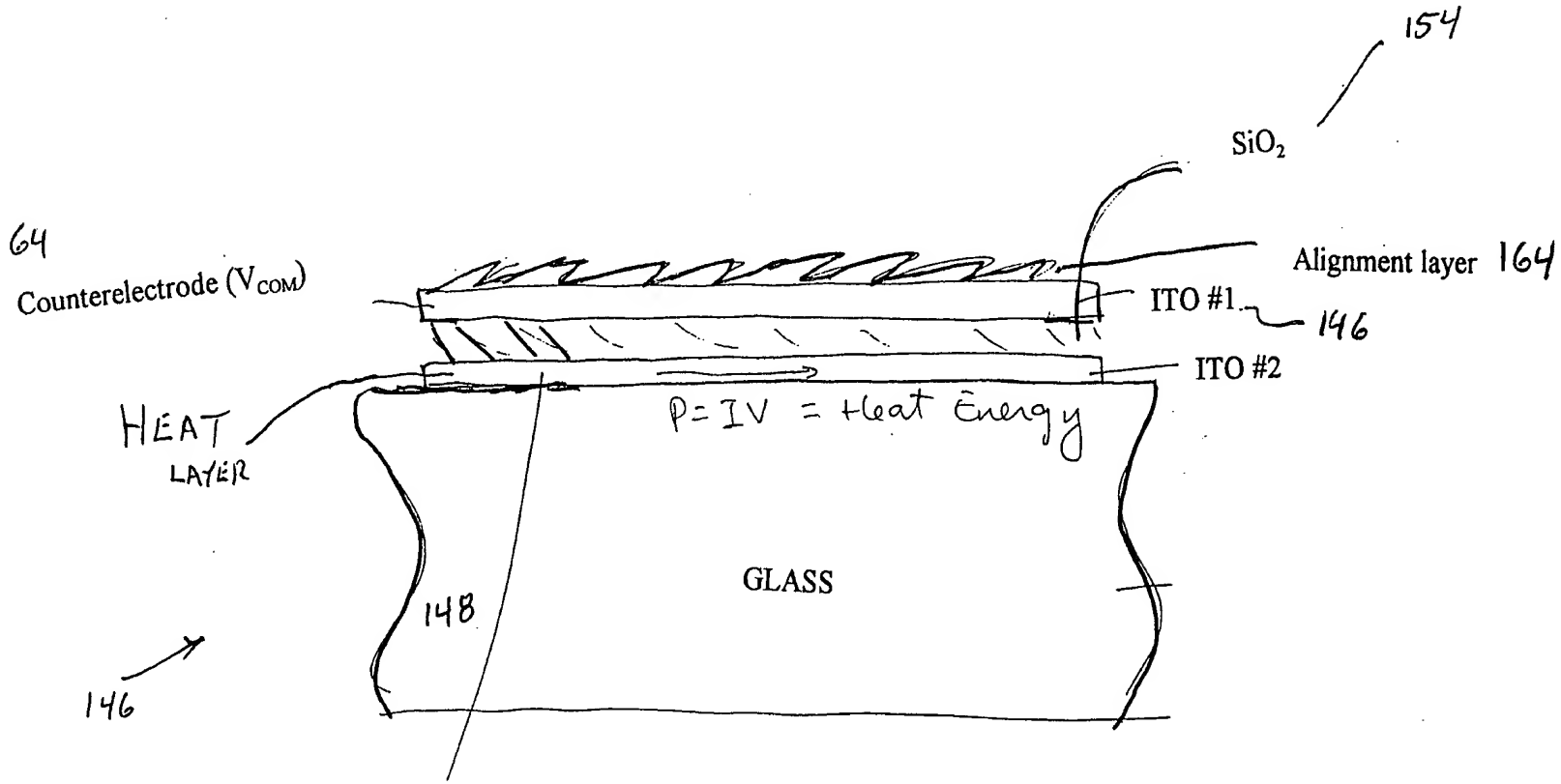


FIGURE 5D



Patterned such that it covering only
the pixel arrays when displayed formed.

FIGURE 6

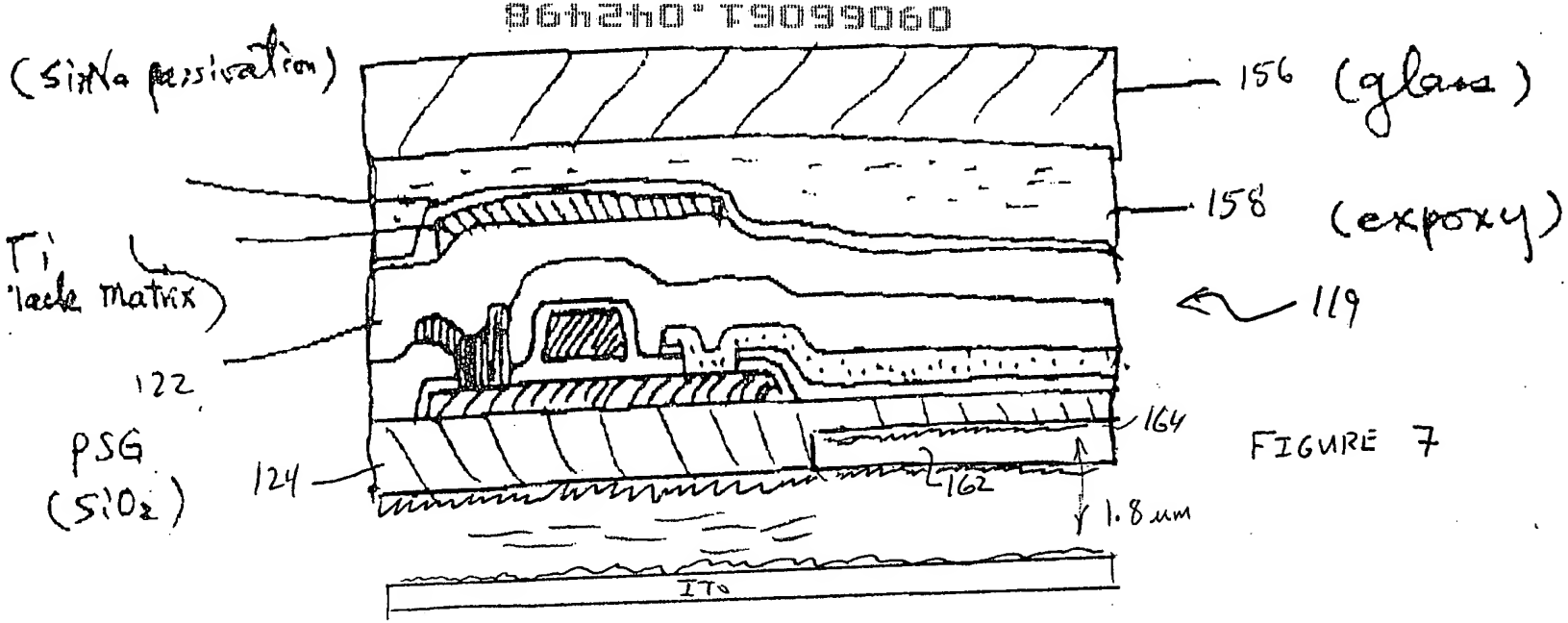


FIGURE 7

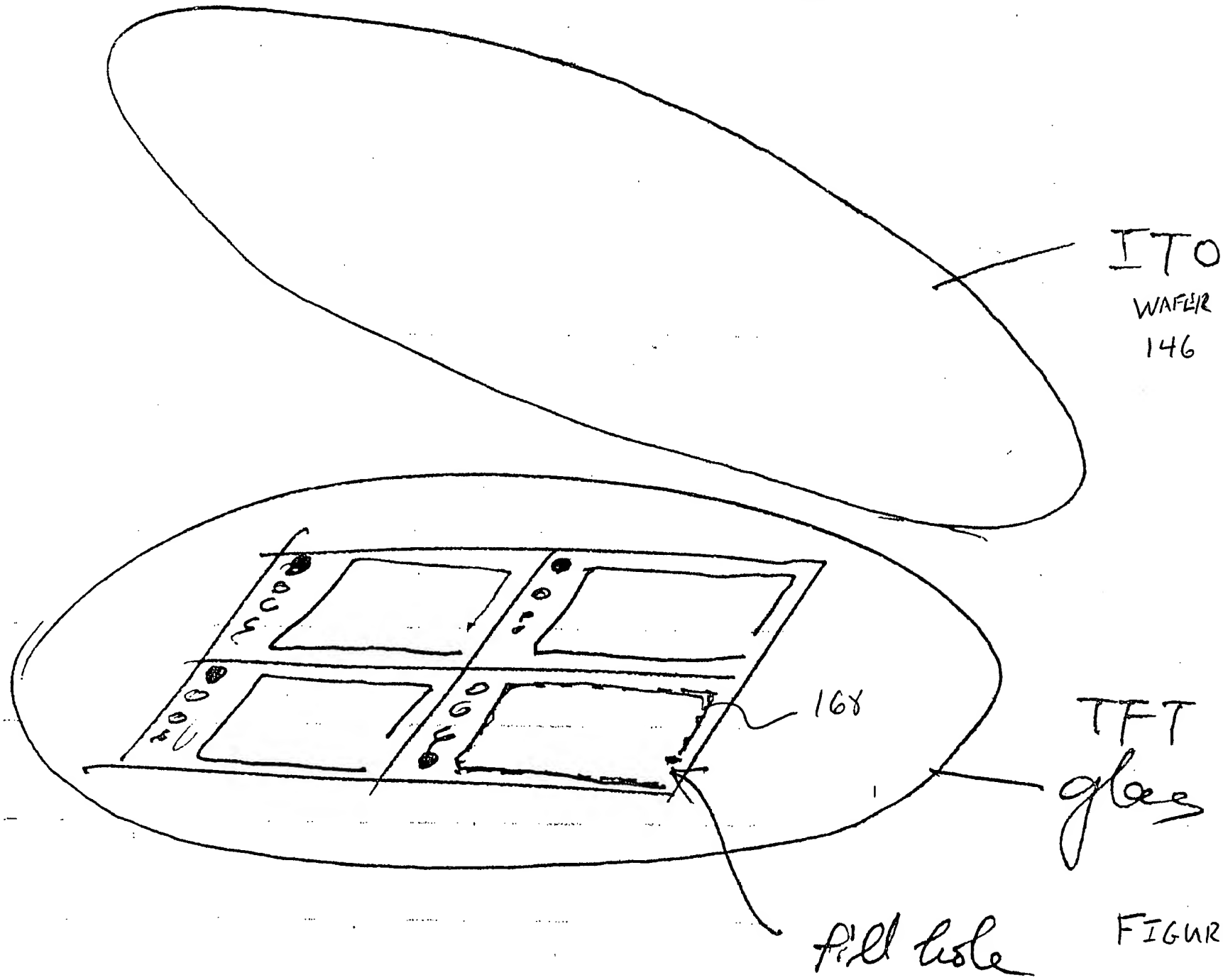


FIGURE 8

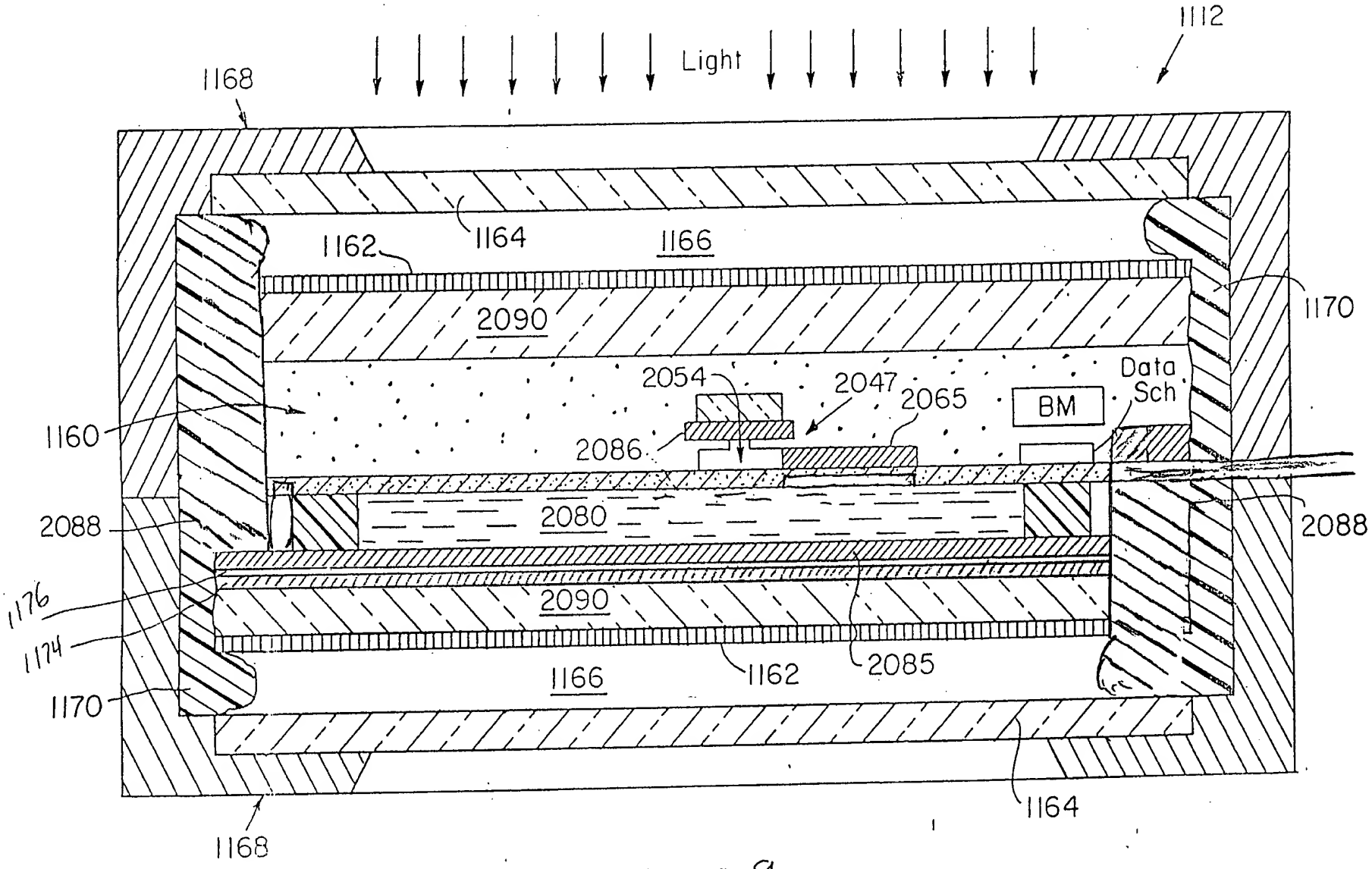

1112
Light
1168
1164
1166
1162
1170
2090
2054
2047
2065
BM
Data
Sch
1160
2086
2088
2080
2088
1176
2090
1174
1162
2085
1166
1170
1164
1168

FIGURE 9

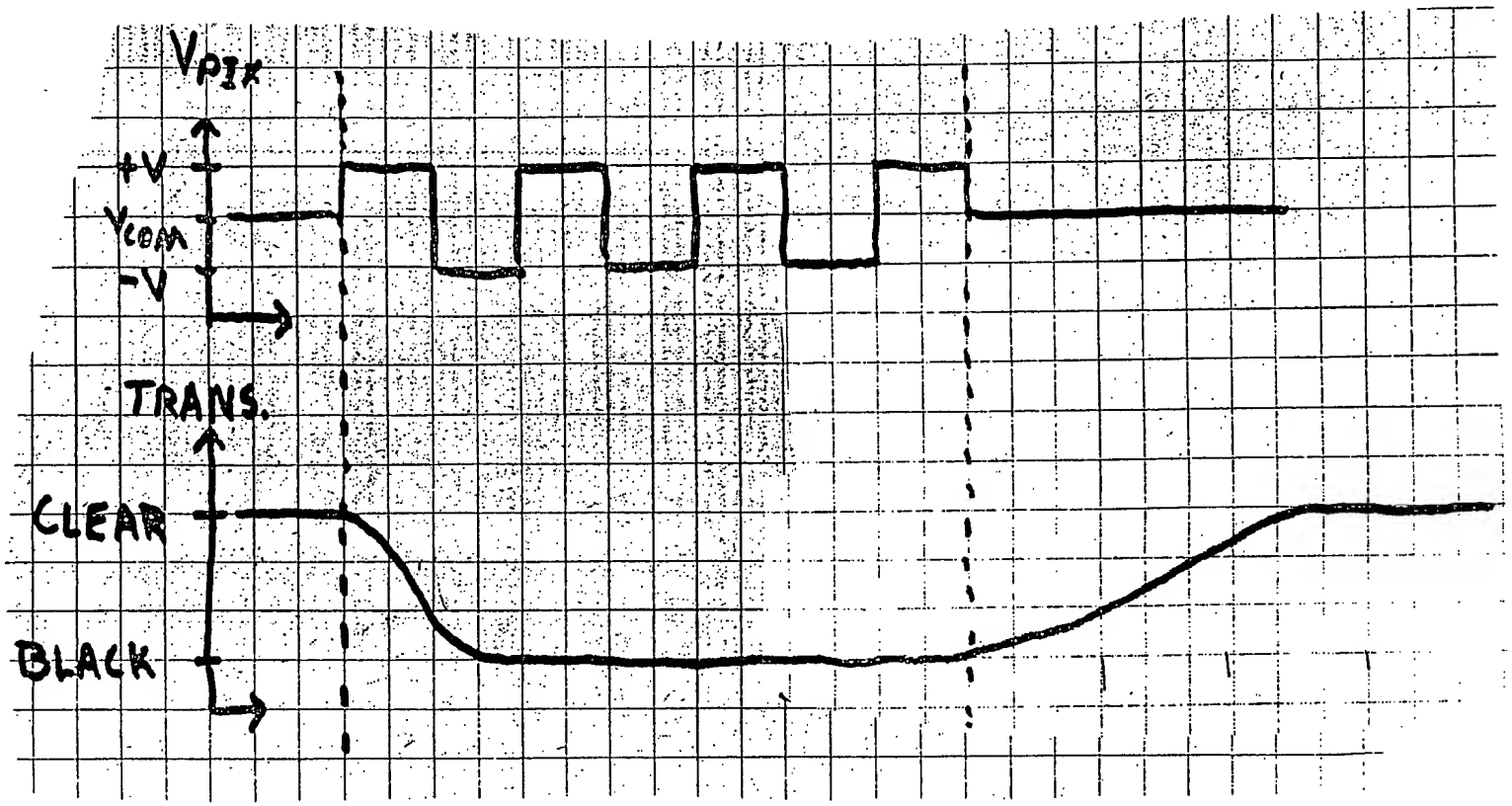


FIGURE 10

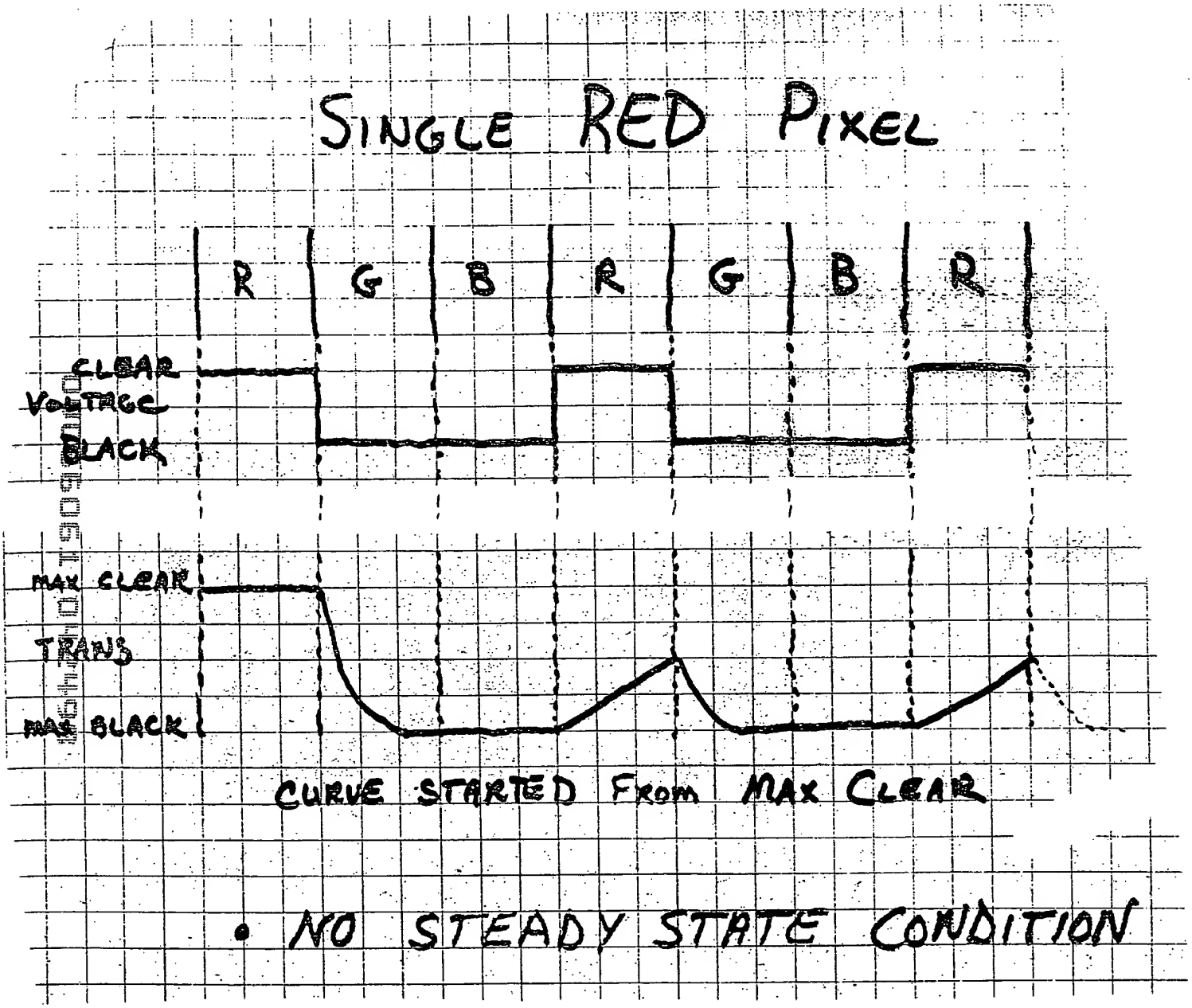
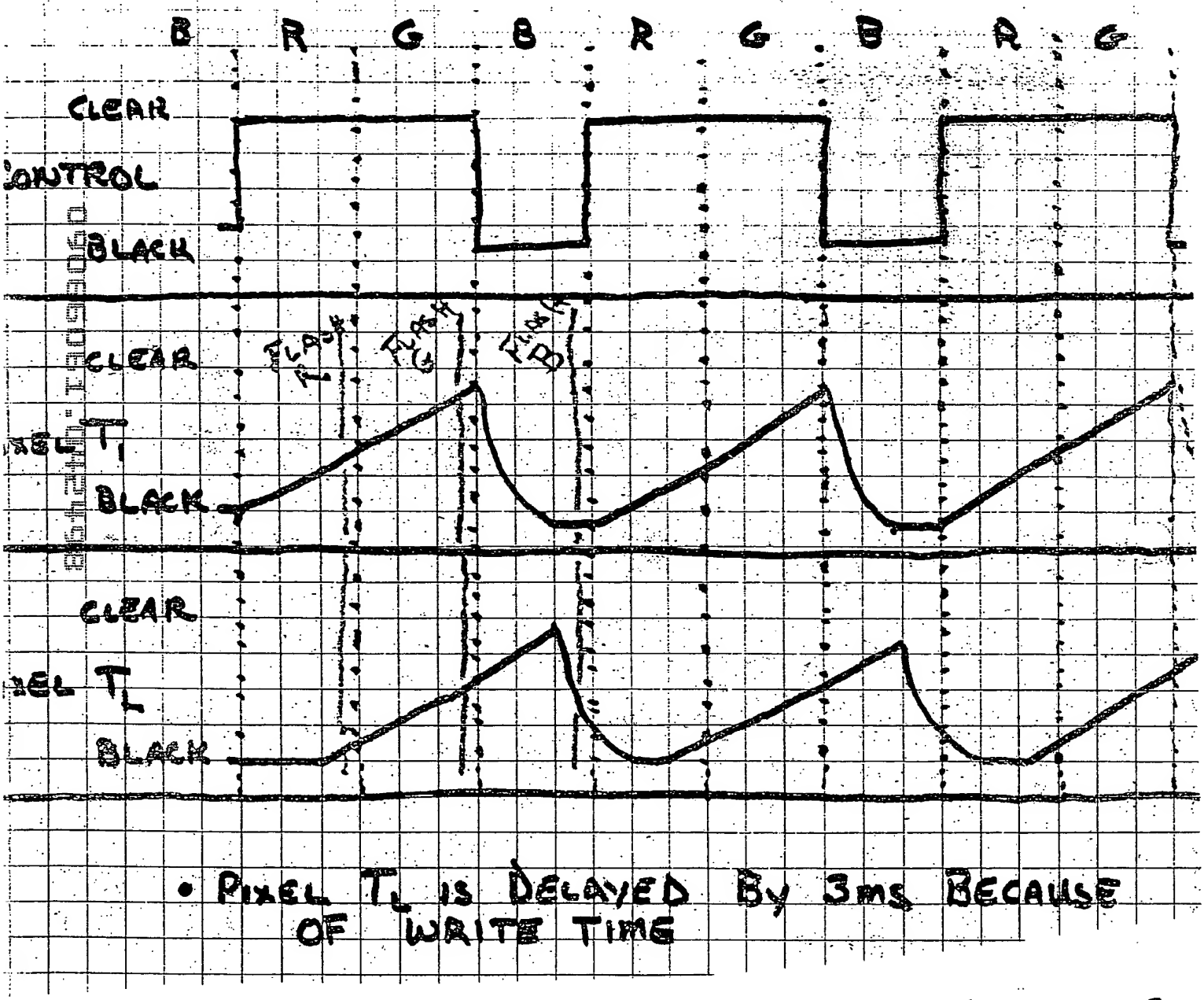

SINGLE RED PIXEL
R
G
B
R
G
B
R
CLEAR VOLTAGE
BLACK
MAX CLEAR
TRANS
MAX BLACK
CURVE STARTED FROM MAX CLEAR
• NO STEADY STATE CONDITION

FIGURE IIA

INTERMEDIATE COLOR (RGB MIX) EX: YELLOW



- PIXEL T_L IS DELAYED BY 3ms BECAUSE OF WRITE TIME

FIGURE 11B

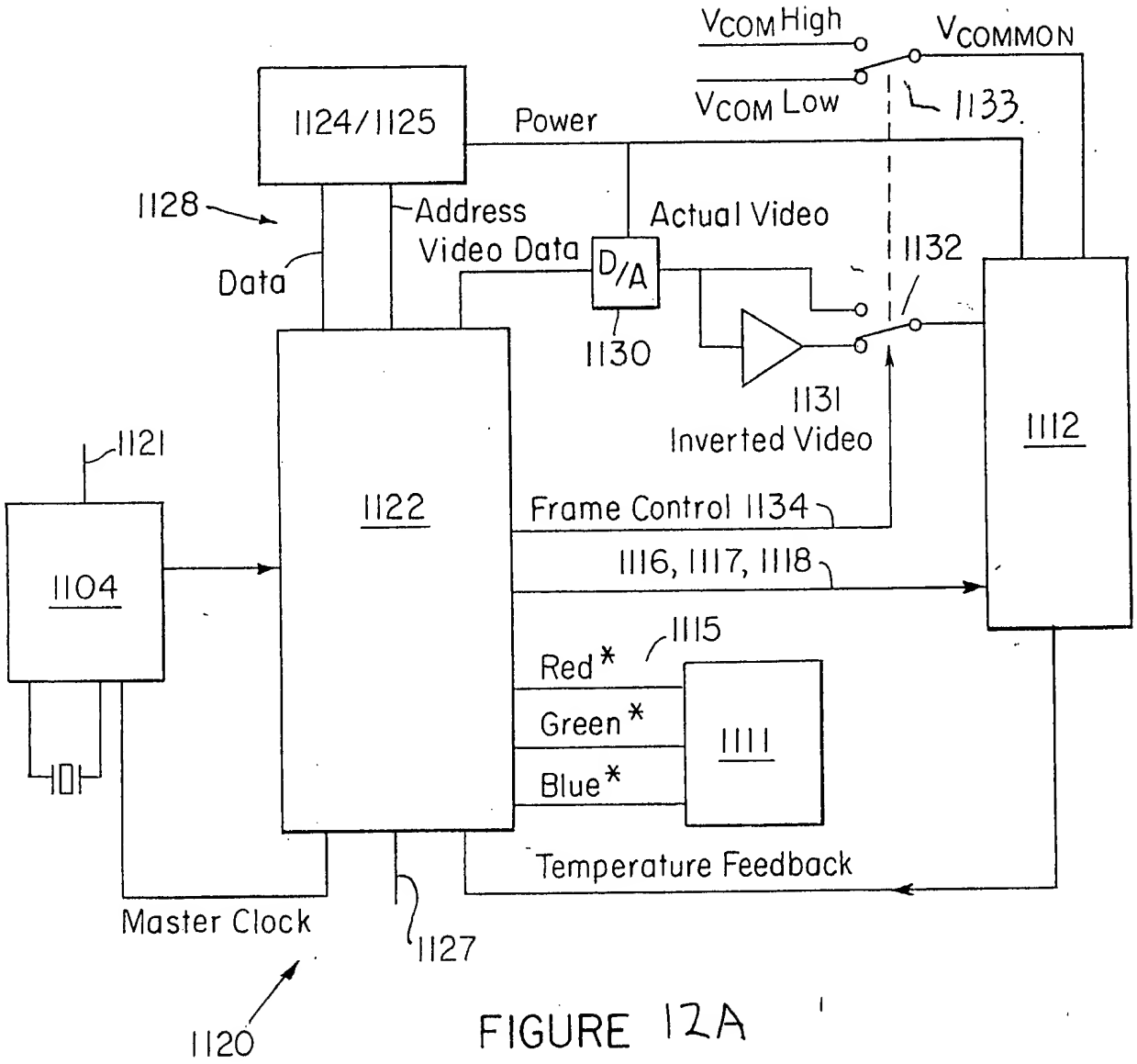

VCOM High
VCOMMON
VCOM Low
1133
1124/1125
Power
1128
Address
Video Data
Actual Video
Data
D/A
1132
1130
1131
Inverted Video
1112
1121
1122
Frame Control 1134
1104
1116, 1117, 1118
1115
Red*
Green*
Blue*
1111
Temperature Feedback
Master Clock
1127
1120

FIGURE 12A

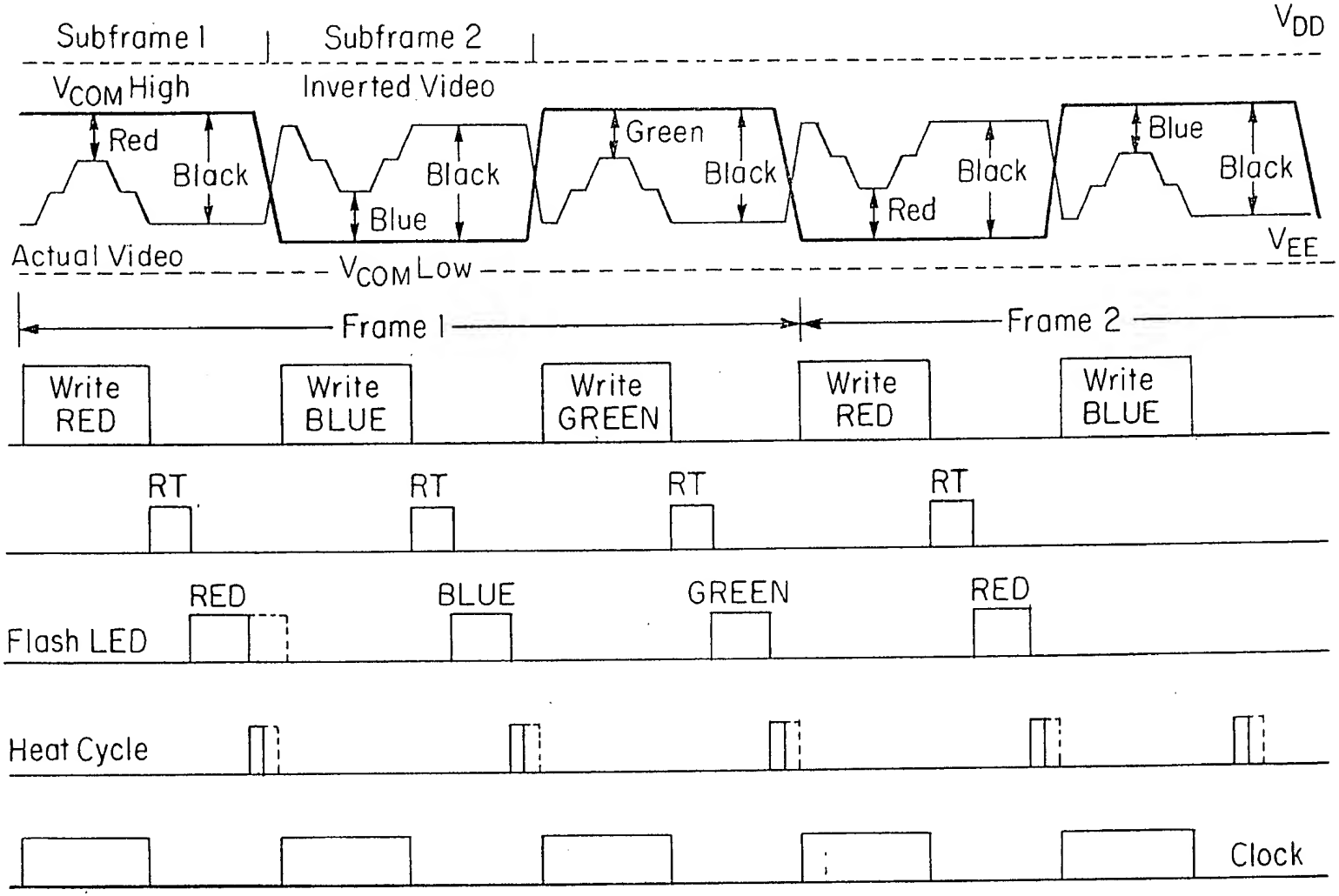

Subframe 1
Subframe 2
V_{DD}
V_{COM} High
Inverted Video
Red
Black
Black
Blue
Black
Green
Black
Red
Black
Blue
Black
Actual Video
V_{COM} Low
V_{EE}
Frame 1
Frame 2
Write RED
Write BLUE
Write GREEN
Write RED
Write BLUE
RT
RT
RT
RT
RED
BLUE
GREEN
RED
Flash LED
Heat Cycle
Clock

FIGURE 12B

Vcom Modulation

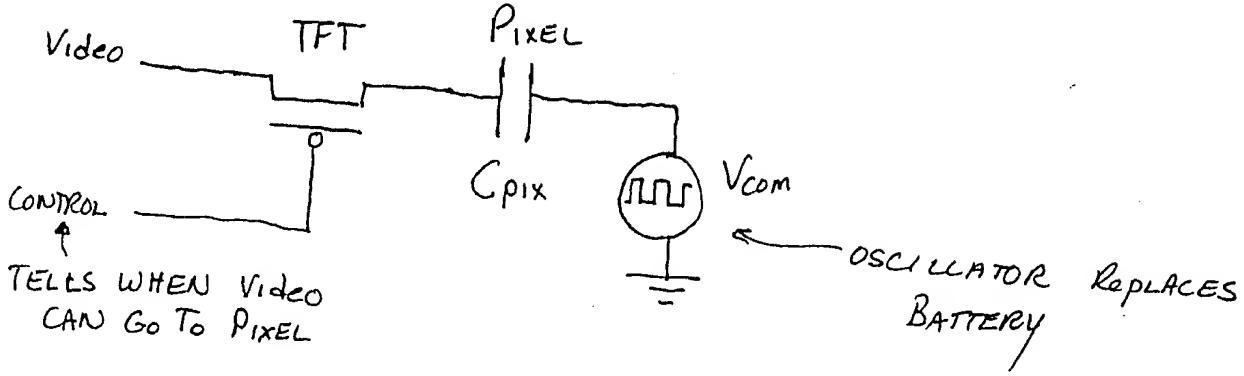


FIGURE 12C

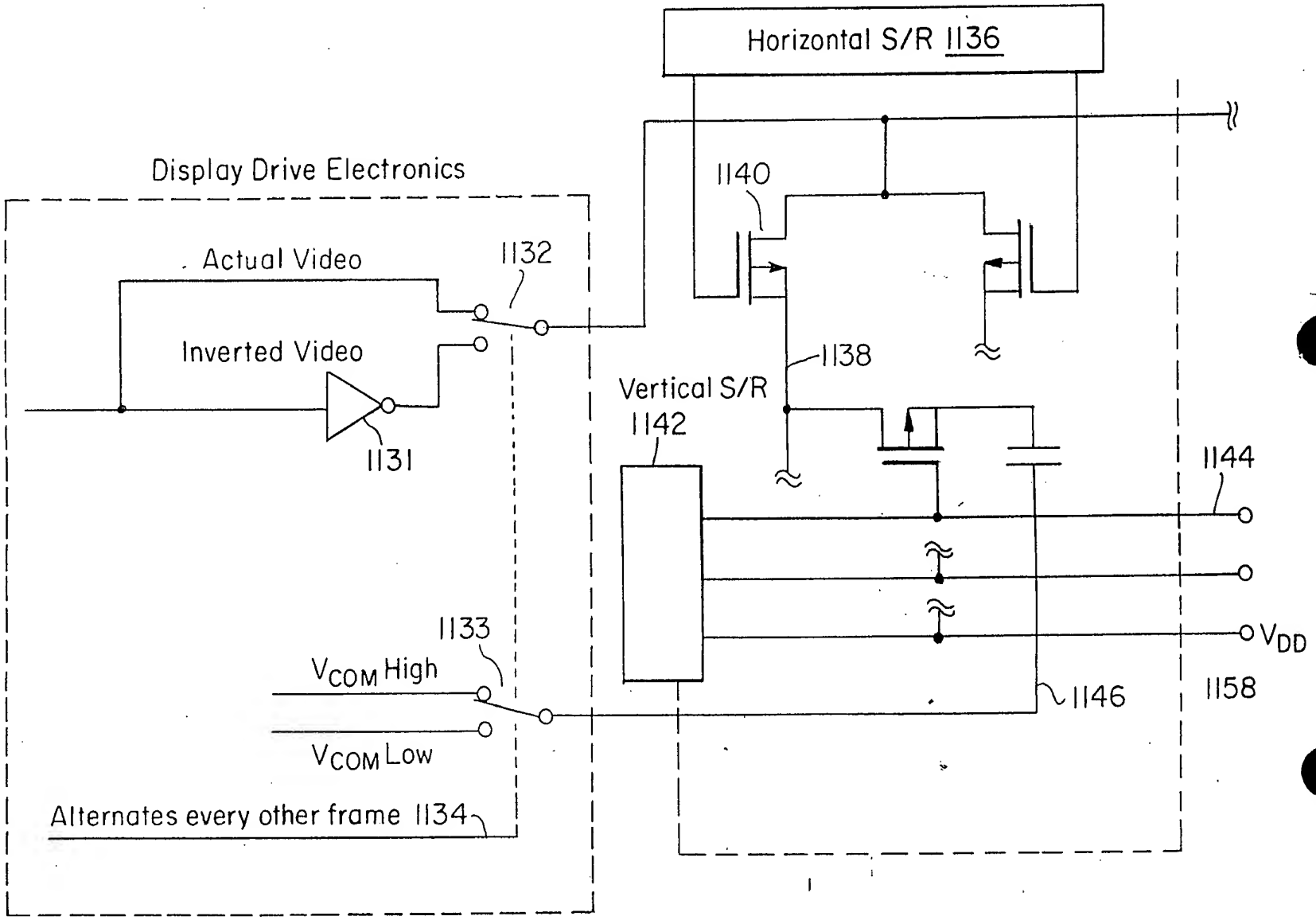


FIGURE 12D

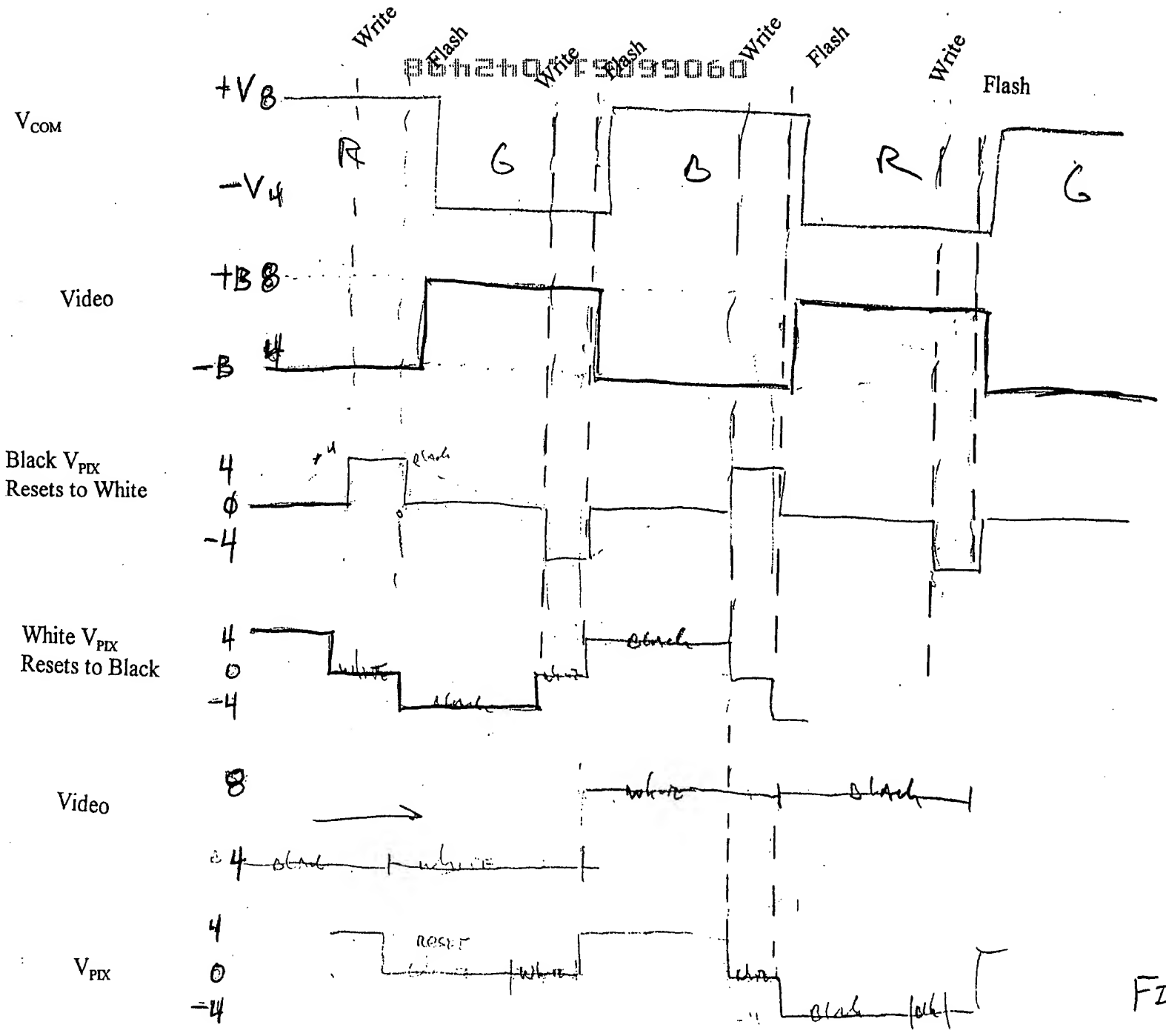

Write
Flash
Write
Flash
Write
Flash
Write
Flash
V_{COM}
$+V_B$
$-V_4$
R
G
B
R
G
Video
$+B_B$
$-B_4$
Black V_{PIX}
Resets to White
4
0
-4
Flash
White V_{PIX}
Resets to Black
4
0
-4
Video
8
4
V_{PIX}
4
0
-4
RESET

FIGURE 13

WRITE VIDEO → WAIT LC TWIST → FLASH → RESET

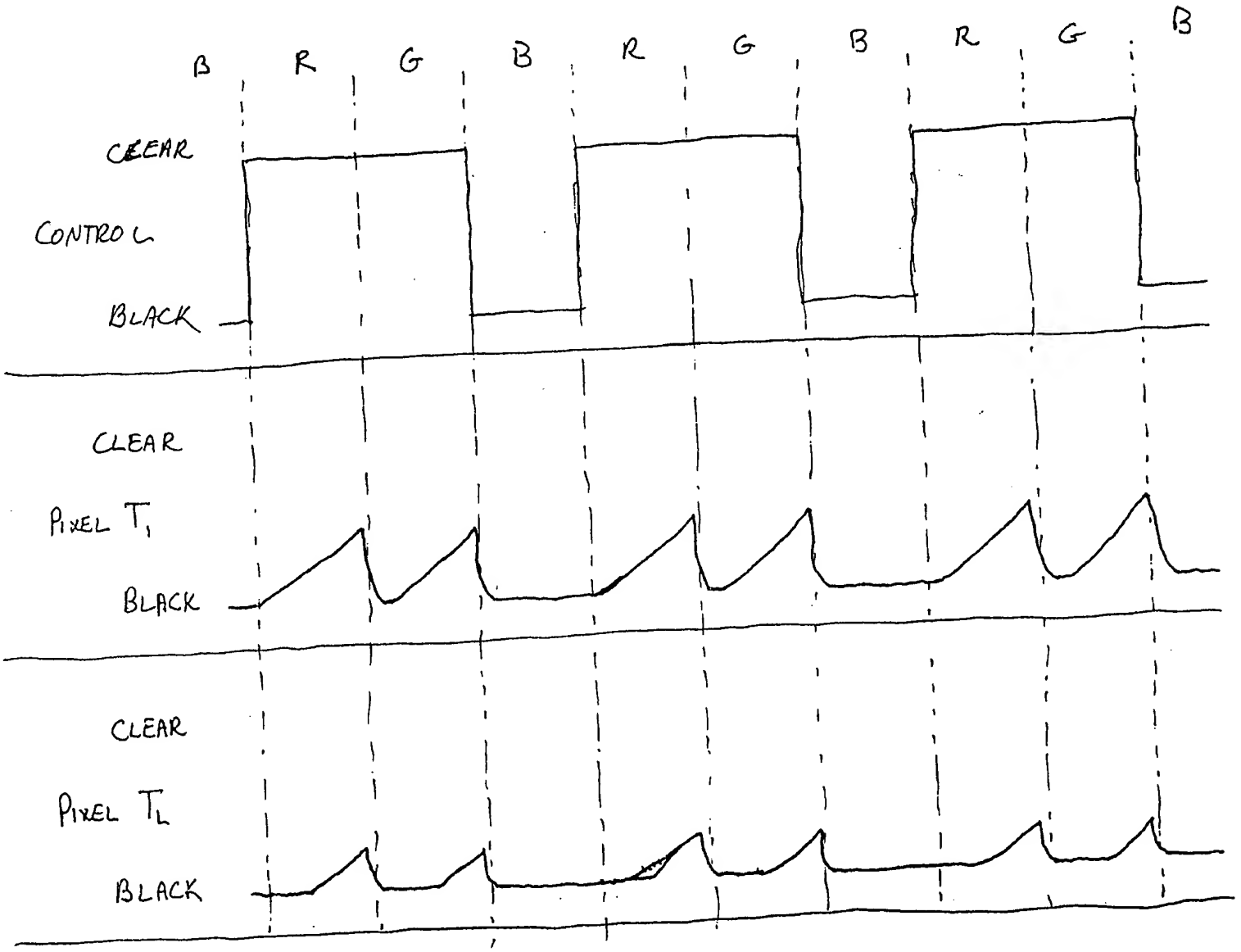


FIGURE 14

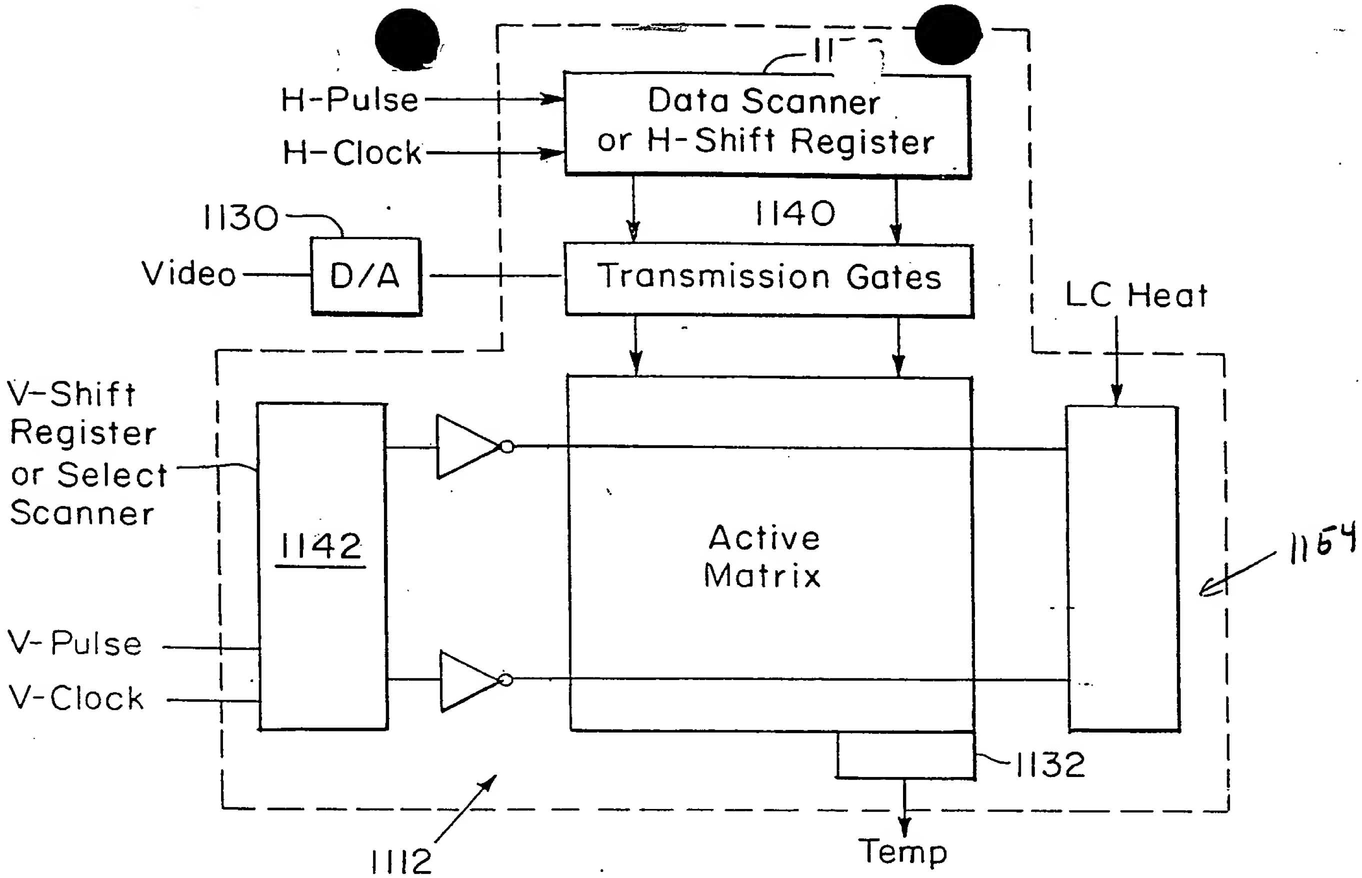


FIGURE 15A

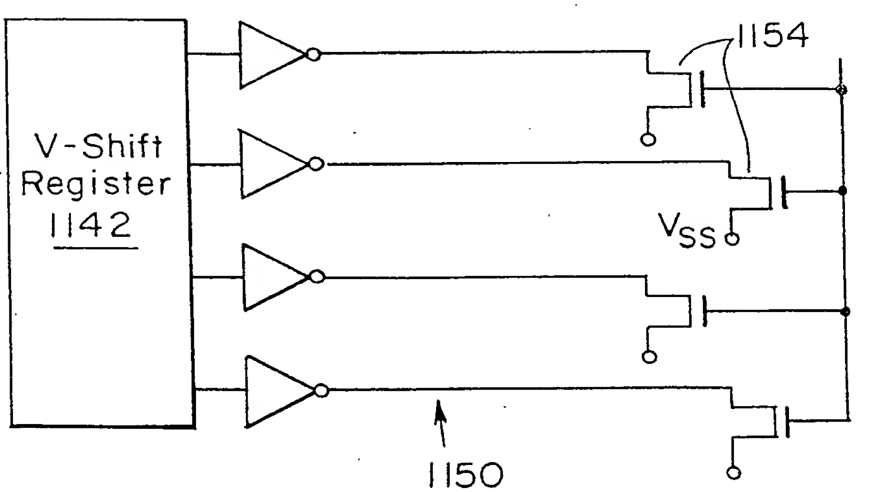


FIGURE 15B

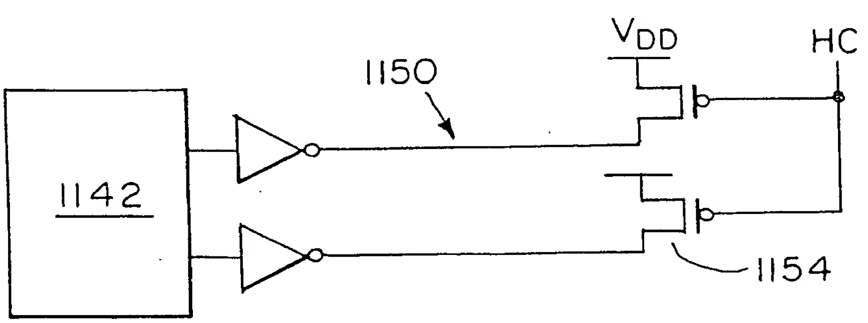


FIGURE 15C

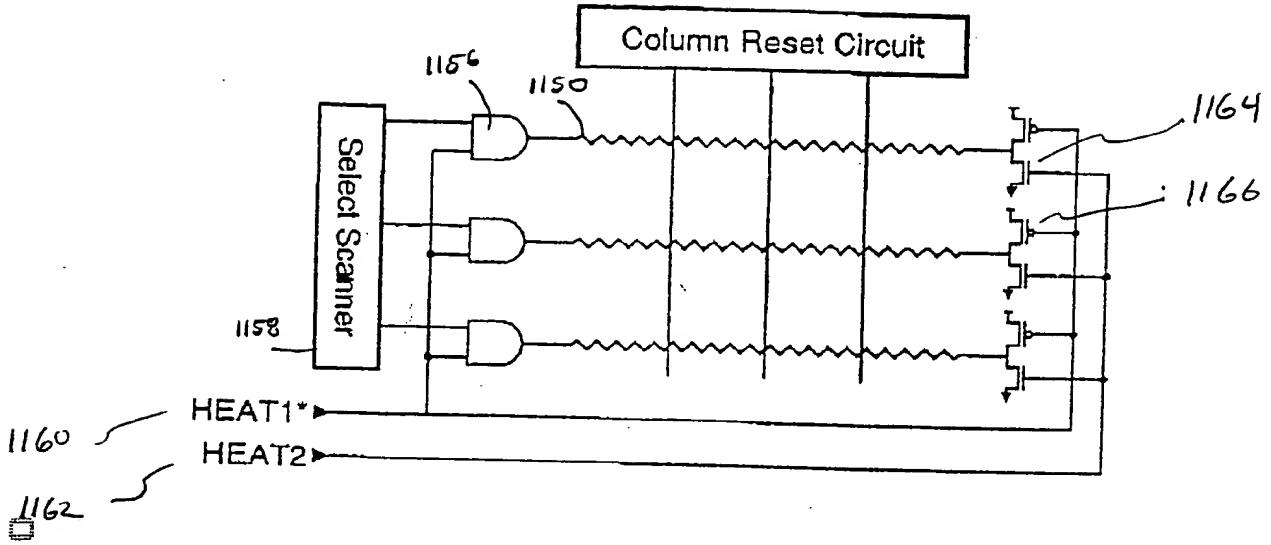


FIGURE 15D

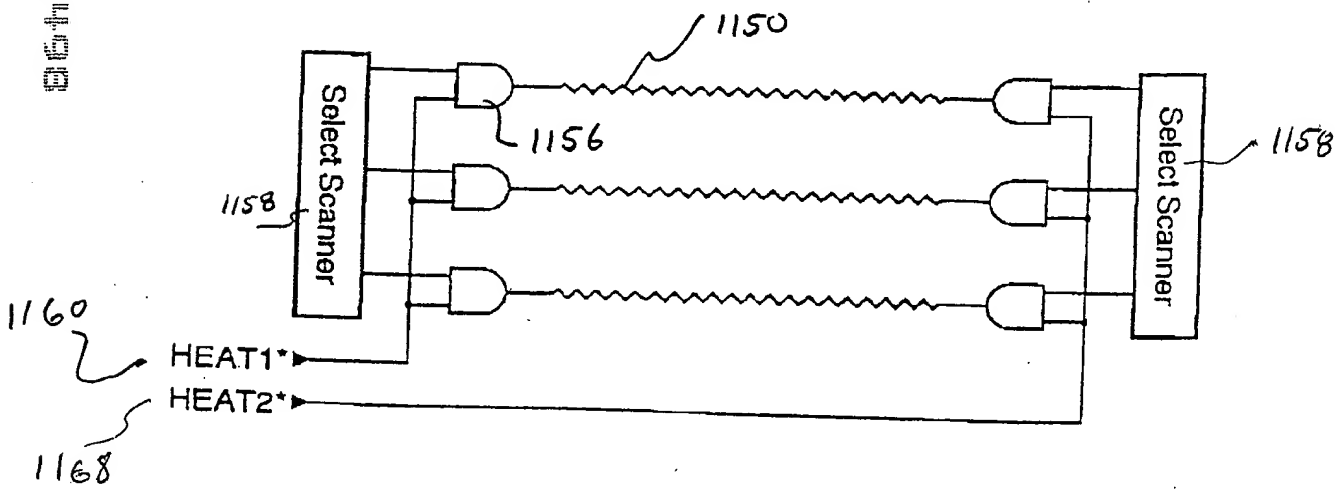


FIGURE 15E

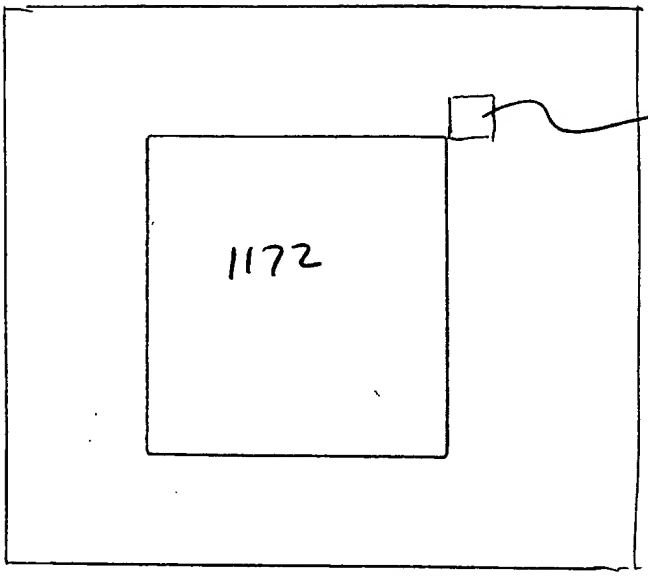


FIGURE 15F

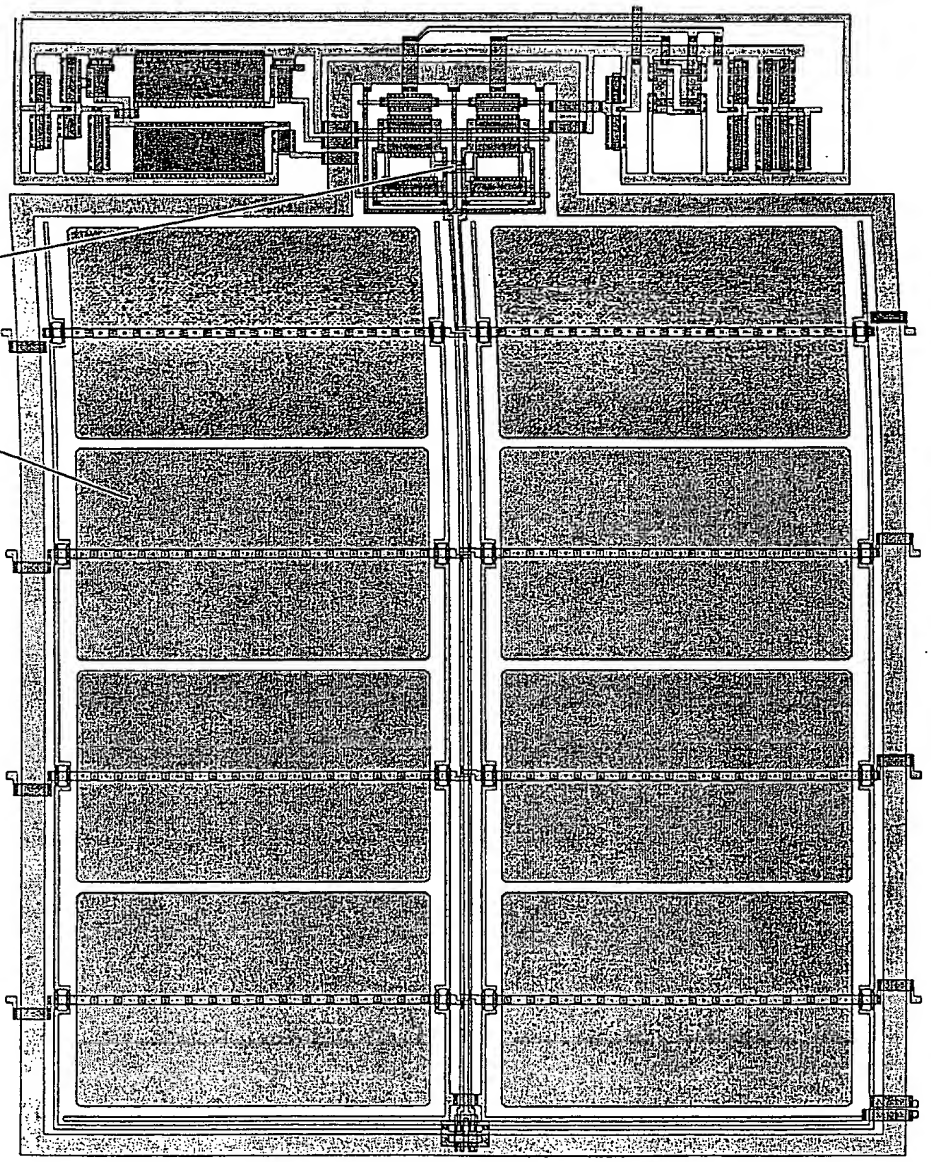


FIGURE 15G

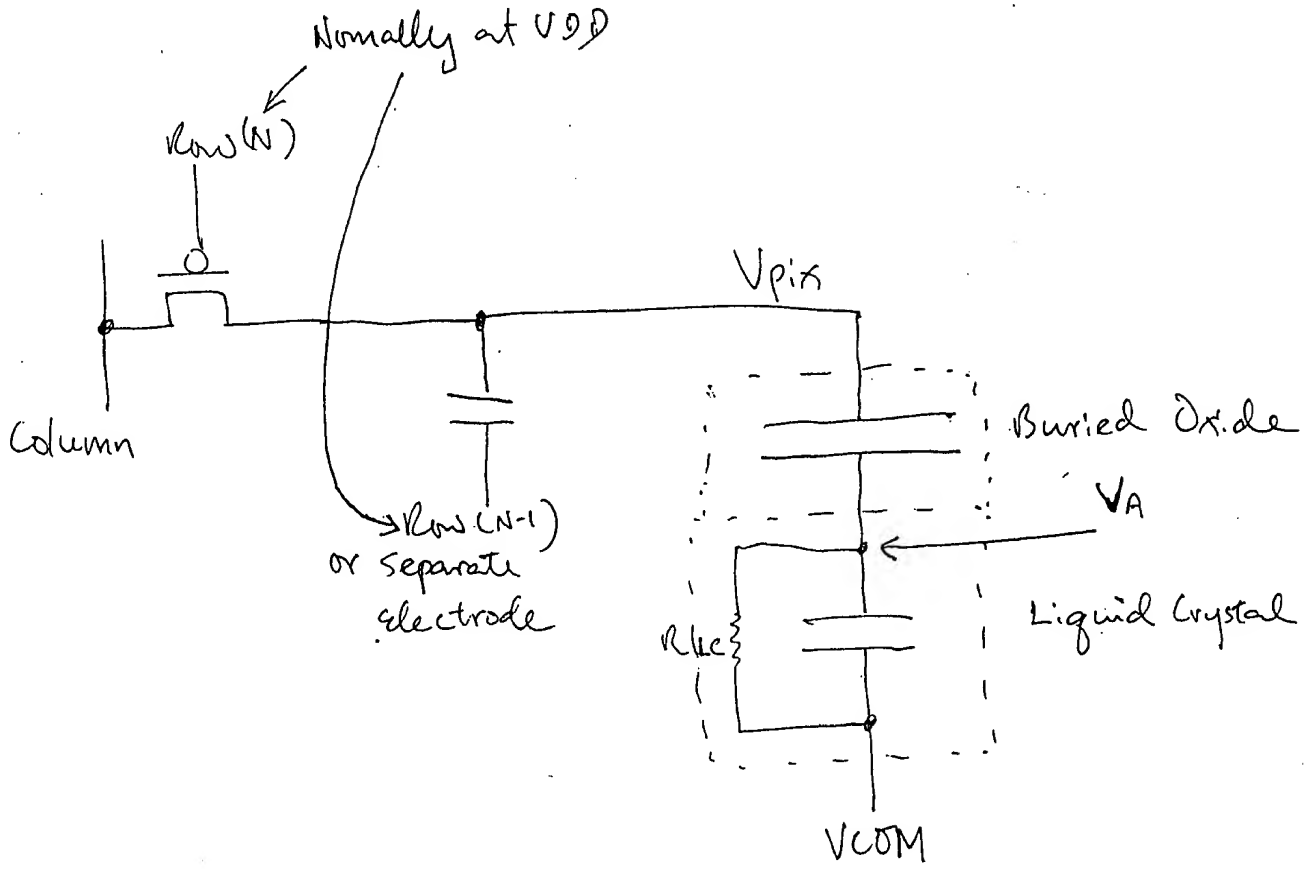

Normally at VDD
Row(N)
Vpix
Column
Buried Oxide
VA
Row(N-1)
or separate
electrode
Liquid Crystal
RLC
VCOM

FIGURE 16

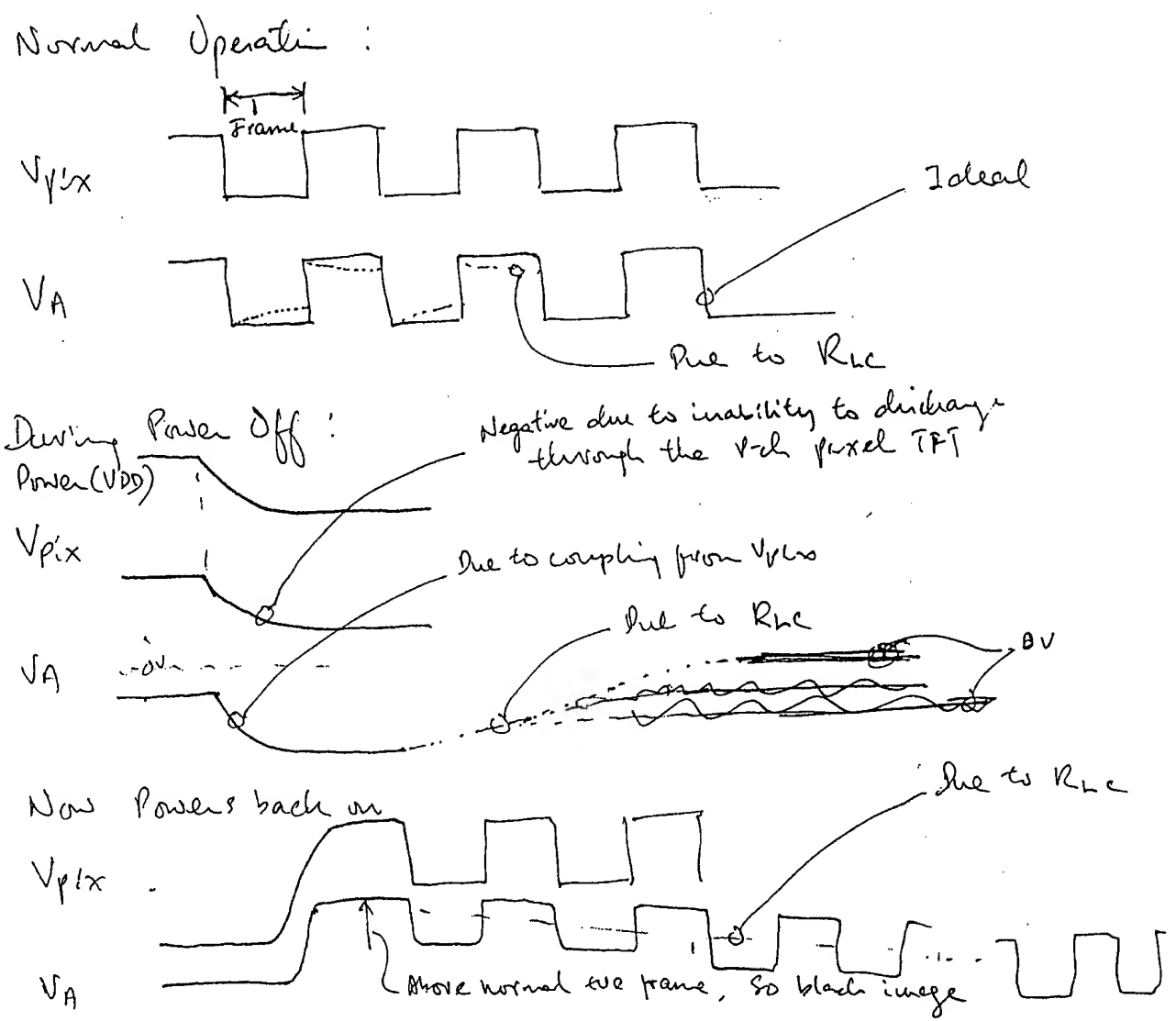

Normal Operation :
Frame
Vpix
Ideal
VA
Due to RLC
During Power Off :
Negative due to inability to discharge through the n-ch pixel TFT
Power (VDD)
Vpix
Due to coupling from Vpix
Due to RLC
VA
0V
BV
Now Power's back on
Due to RLC
Vpix
VA
Above normal two frame, so black image

FIGURE 17

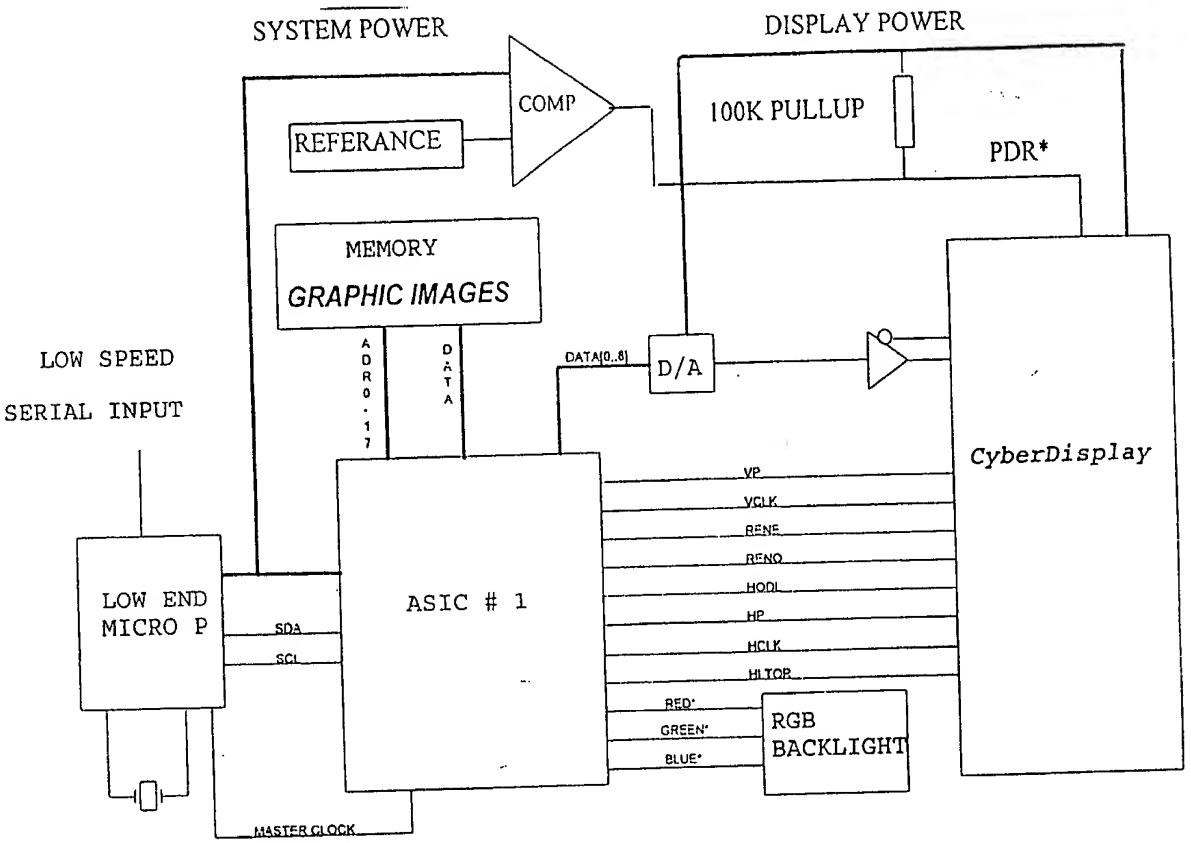

SYSTEM POWER
DISPLAY POWER
COMP
REFERANCE
100K PULLUP
PDR*
MEMORY
GRAPHIC IMAGES
ADR0-17
DATA
DATA[0..8]
D/A
LOW SPEED
SERIAL INPUT
CyberDisplay
VP
VCLK
RENE
RENO
HODL
HP
HCLK
HLTOR
LOW END
MICRO P
SDA
SCL
ASIC # 1
RED*
GREEN*
BLUE*
RGB
BACKLIGHT
MASTER CLOCK

FIGURE 1B

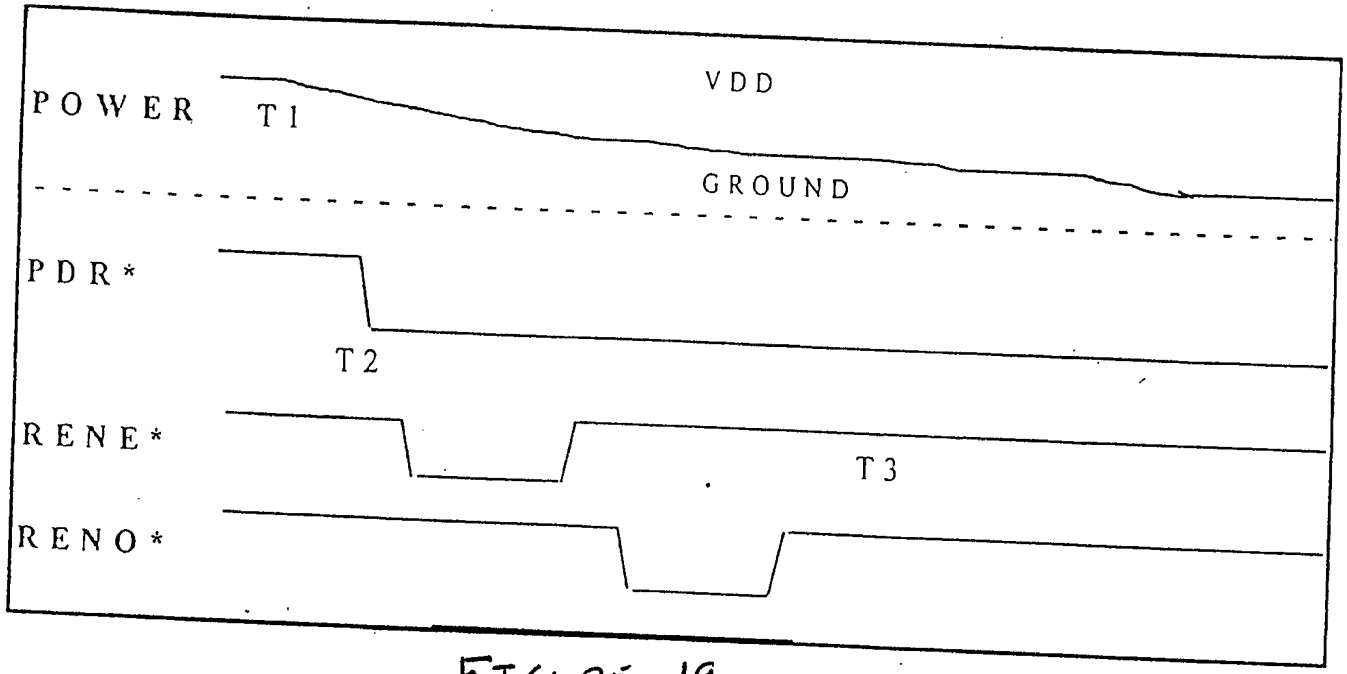


FIGURE 19

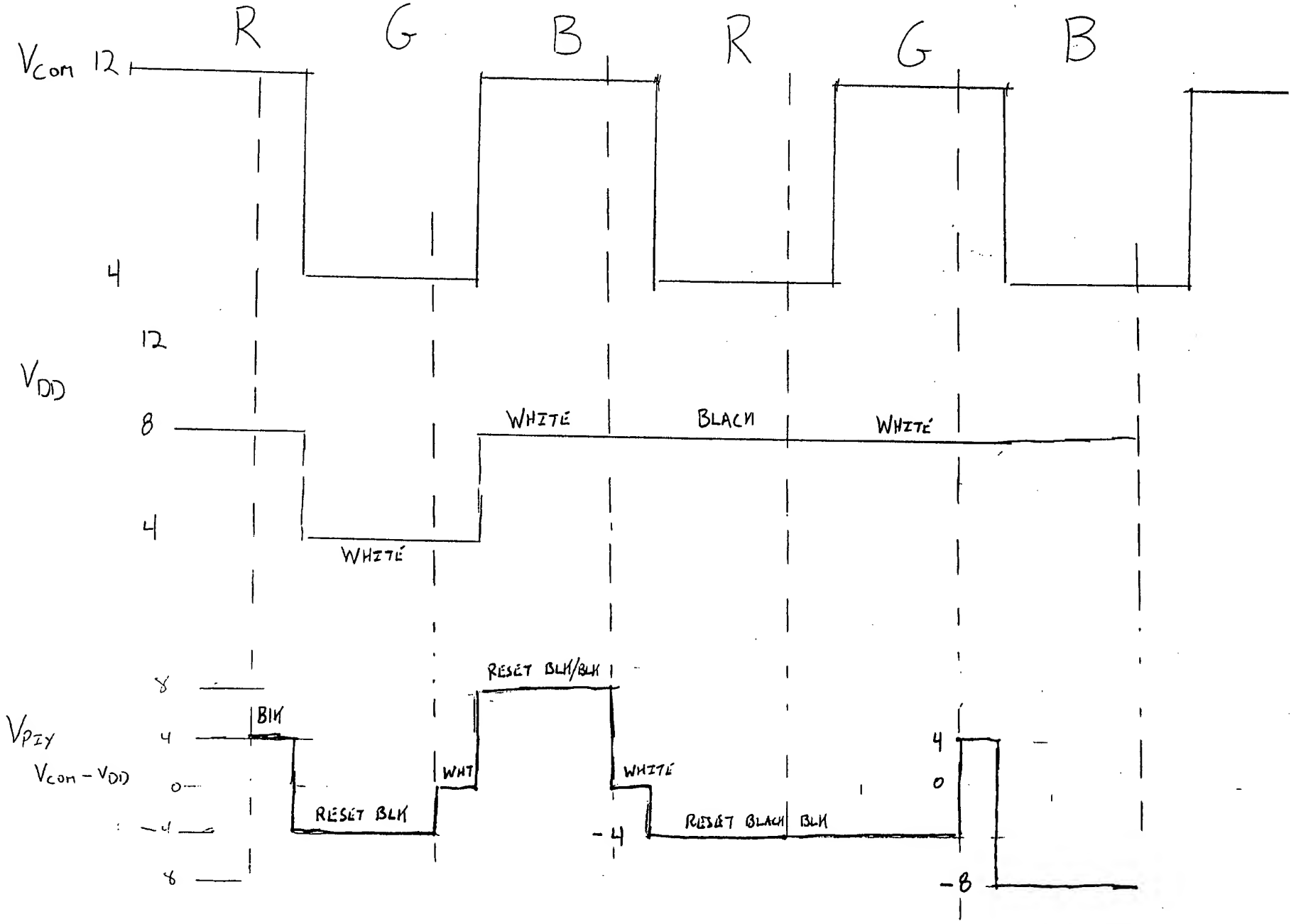


FIGURE 20

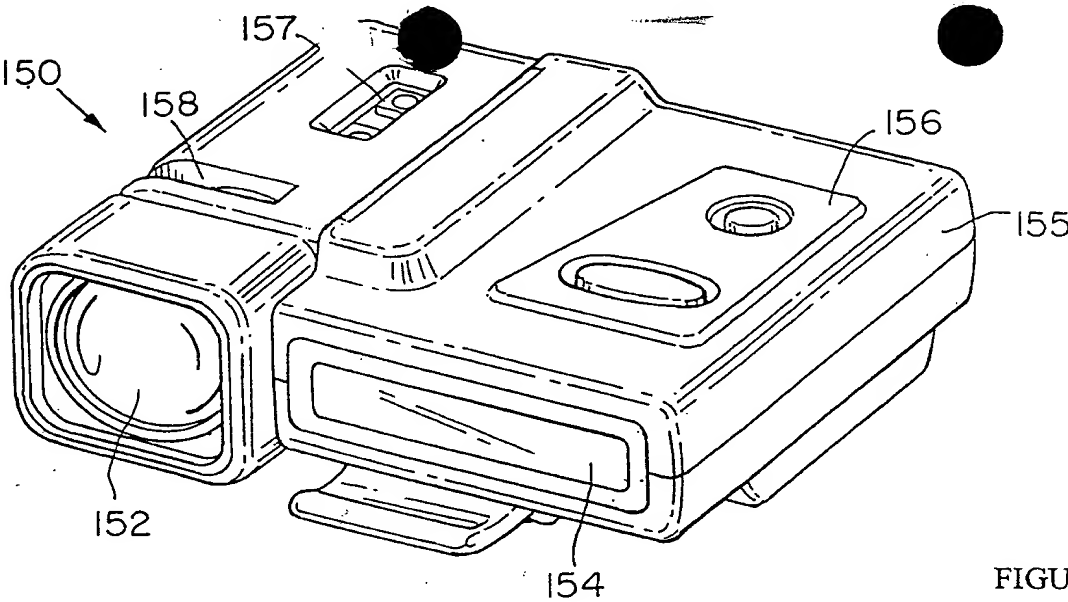


FIGURE 21A

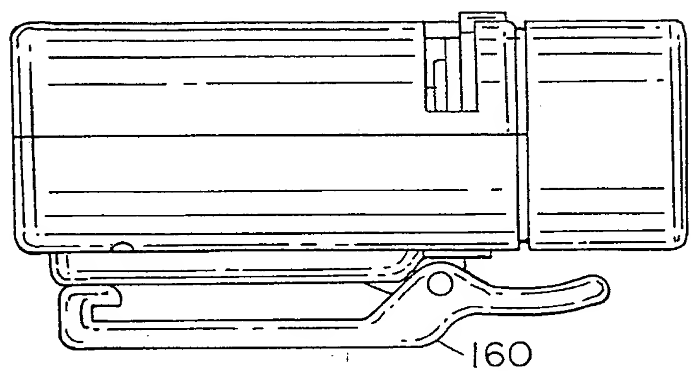


FIGURE 21C

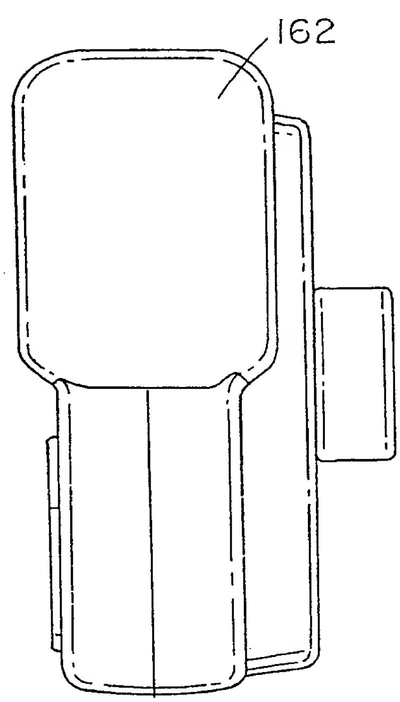


FIGURE 21B

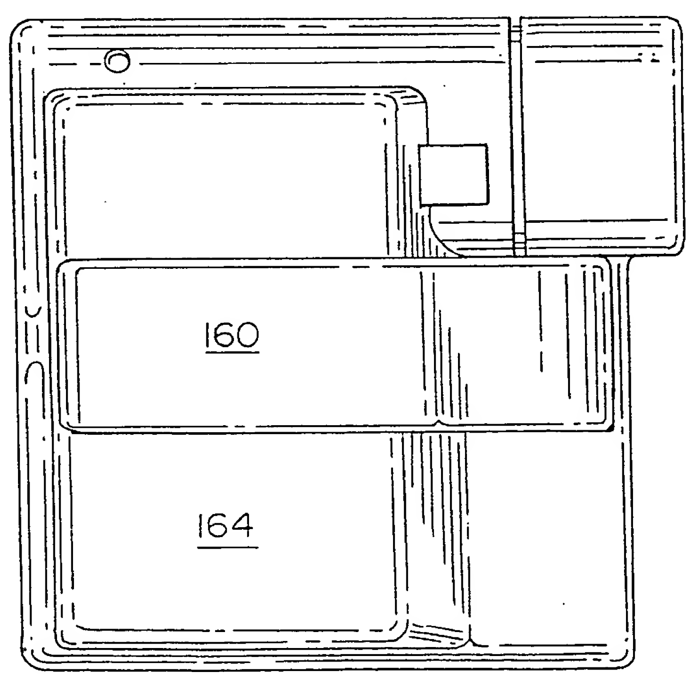


FIGURE 21D

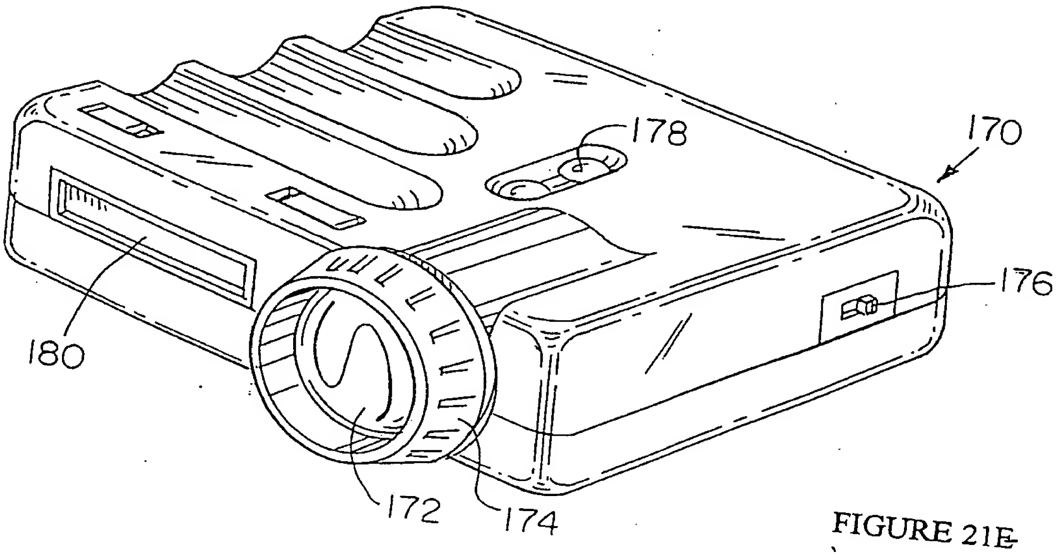


FIGURE 21E

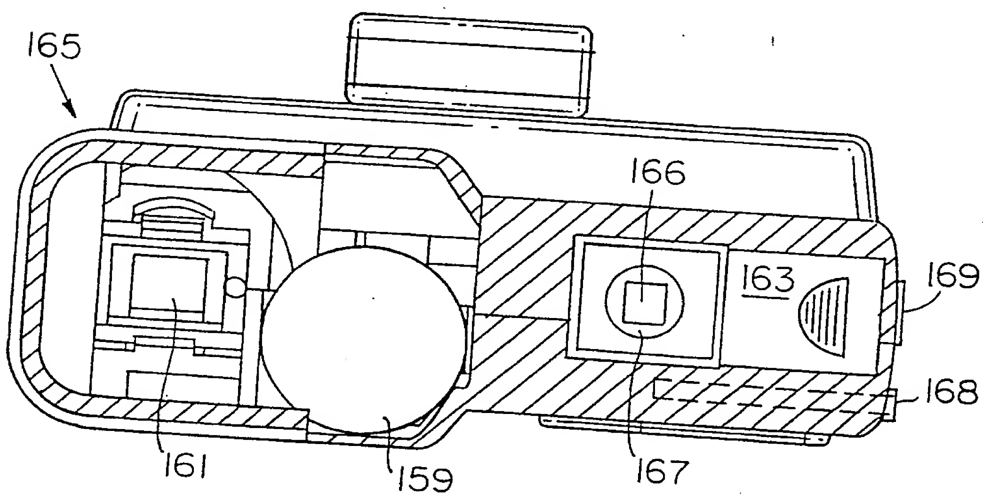


FIGURE 22

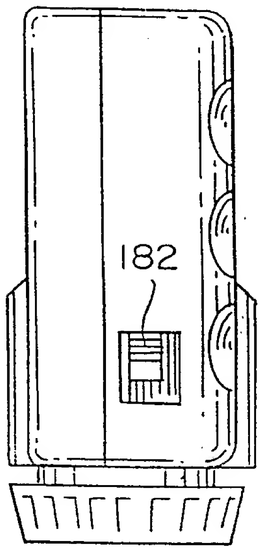


FIGURE 21G

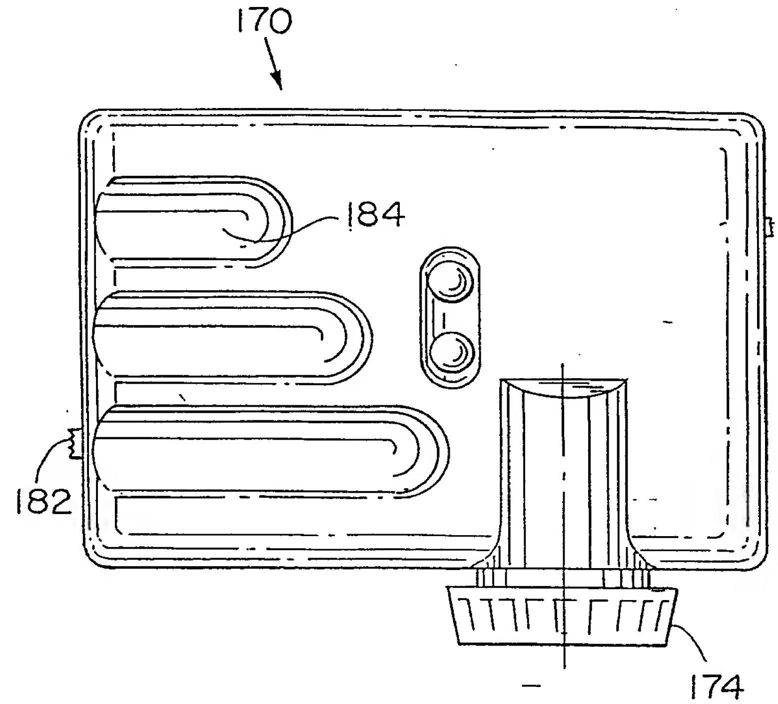


FIGURE 21F

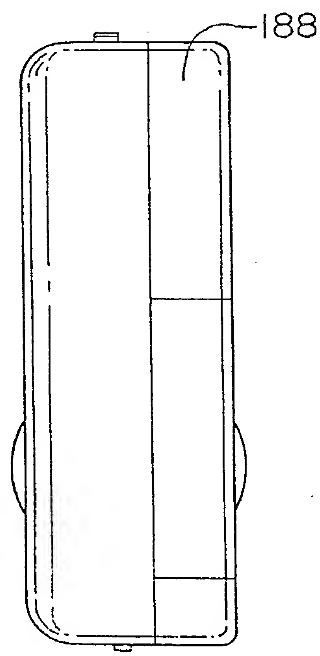


FIGURE 21H

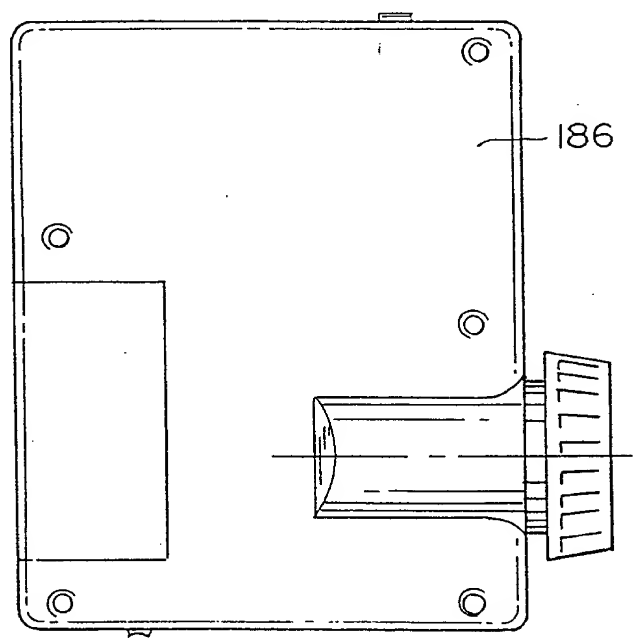
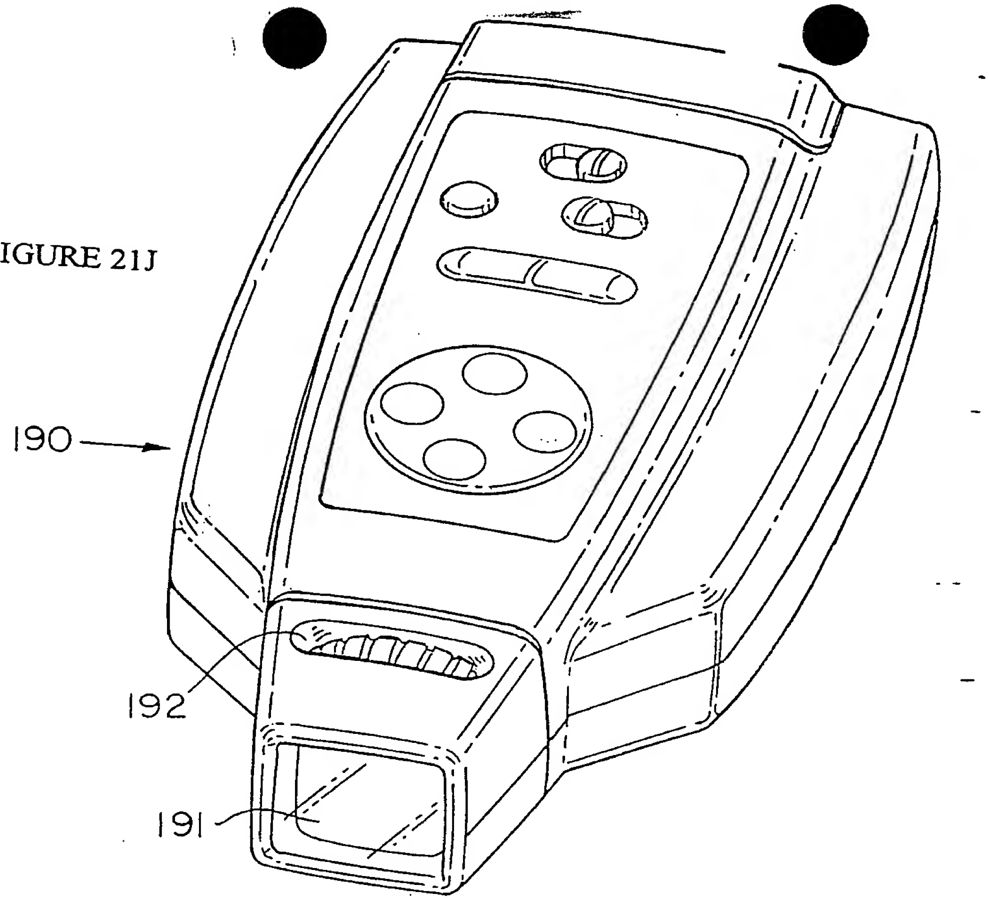


FIGURE 21I

FIGURE 21J



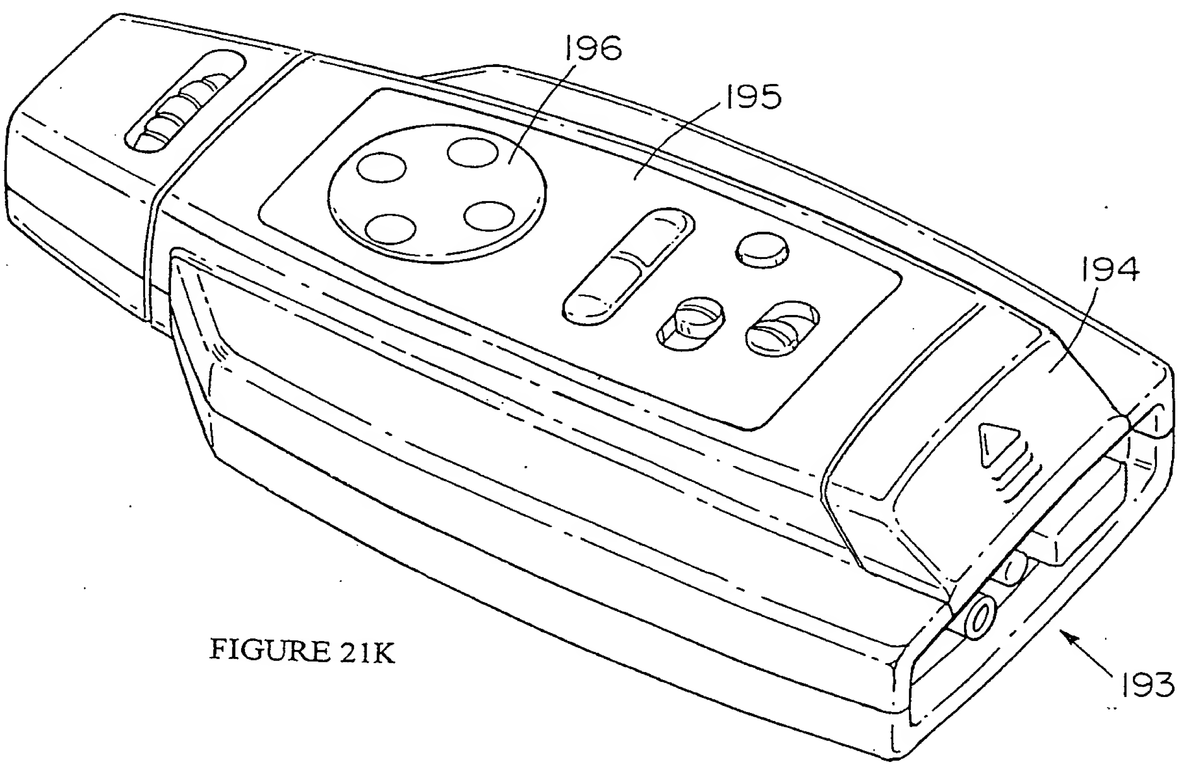


FIGURE 21K

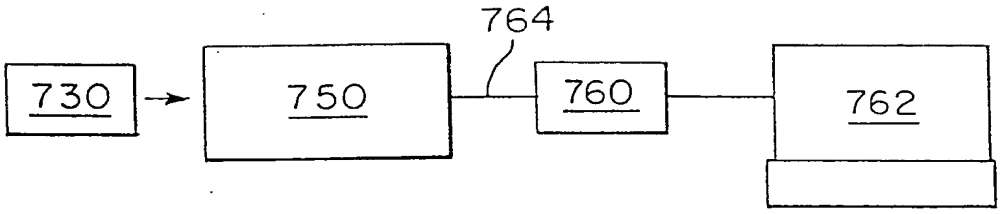


FIGURE 23A

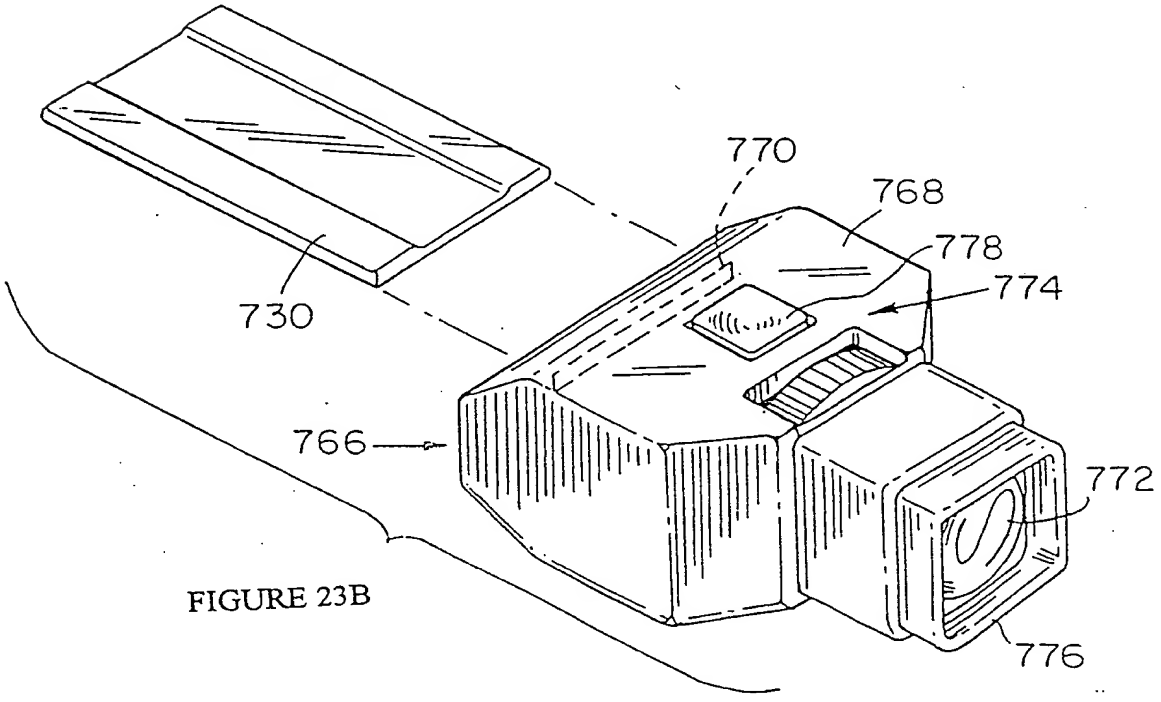


FIGURE 23B

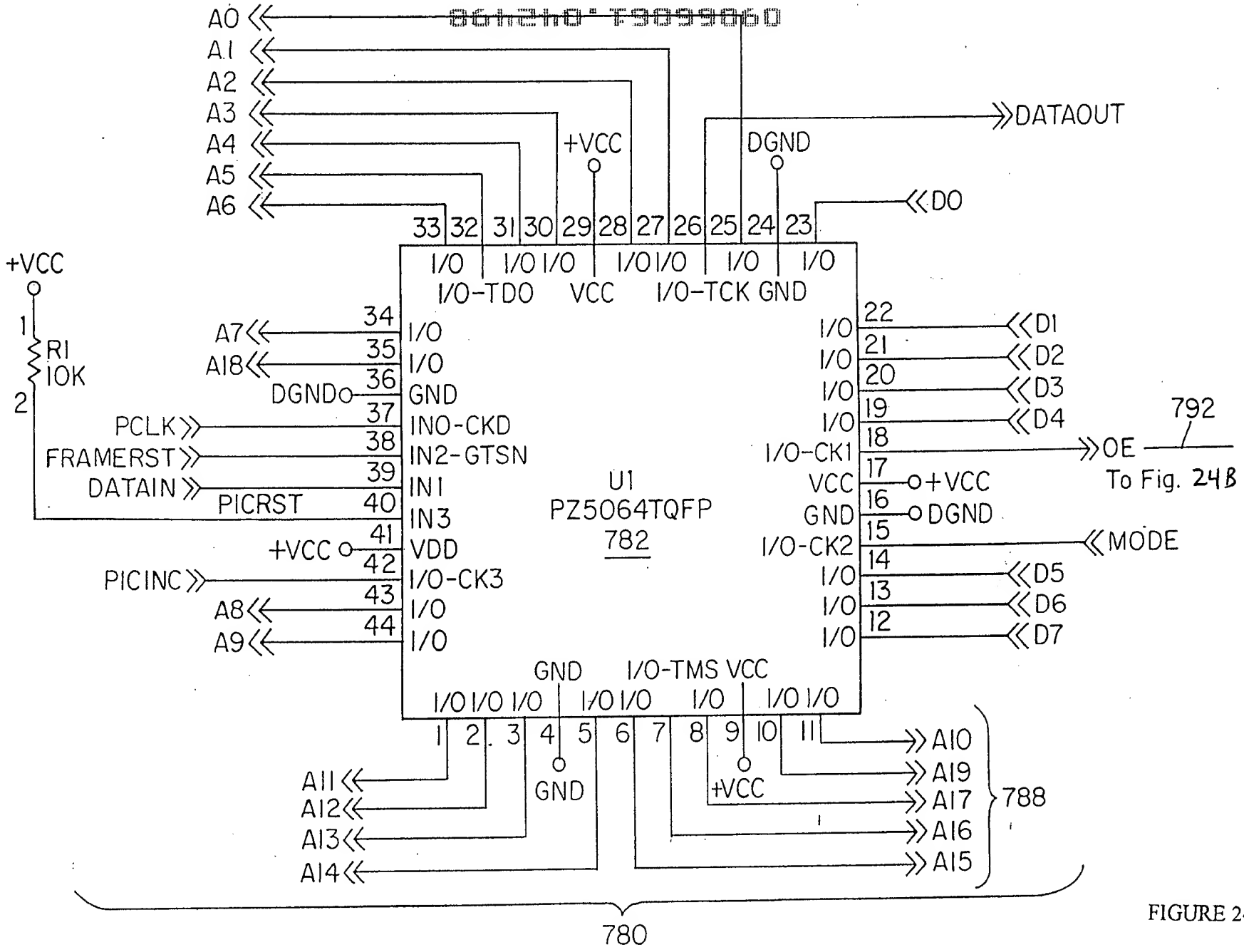

A0
A1
A2
A3
A4
A5
A6
DATAOUT
+VCC
DGND
DO
33 32 31 30 29 28 27 26 25 24 23
I/O I/O I/O I/O I/O I/O I/O
I/O-TDO VCC I/O-TCK GND
+VCC
1
RI
10K
2
A7
A18
DGND
PCLK
FRAMERST
DATAIN
PICRST
34 I/O
35 I/O
36 GND
37 INO-CKD
38 IN2-GTSN
39 IN1
40 IN3
41 VDD
42 I/O-CK3
43 I/O
44 I/O
+VCC
PICINC
A8
A9
U1
PZ5064TQFP
782
22 I/O
21 I/O
20 I/O
19 I/O
18 I/O-CK1
17 VCC
16 GND
15 I/O-CK2
14 I/O
13 I/O
12 I/O
D1
D2
D3
D4
OE
+VCC
DGND
MODE
D5
D6
D7
792
To Fig. 24B
GND I/O-TMS VCC
I/O I/O I/O I/O I/O I/O I/O I/O I/O
1 2 3 4 5 6 7 8 9 10 11
A11
A12
A13
A14
GND
+VCC
A10
A19
A17
A16
A15
788
780

FIGURE 24A

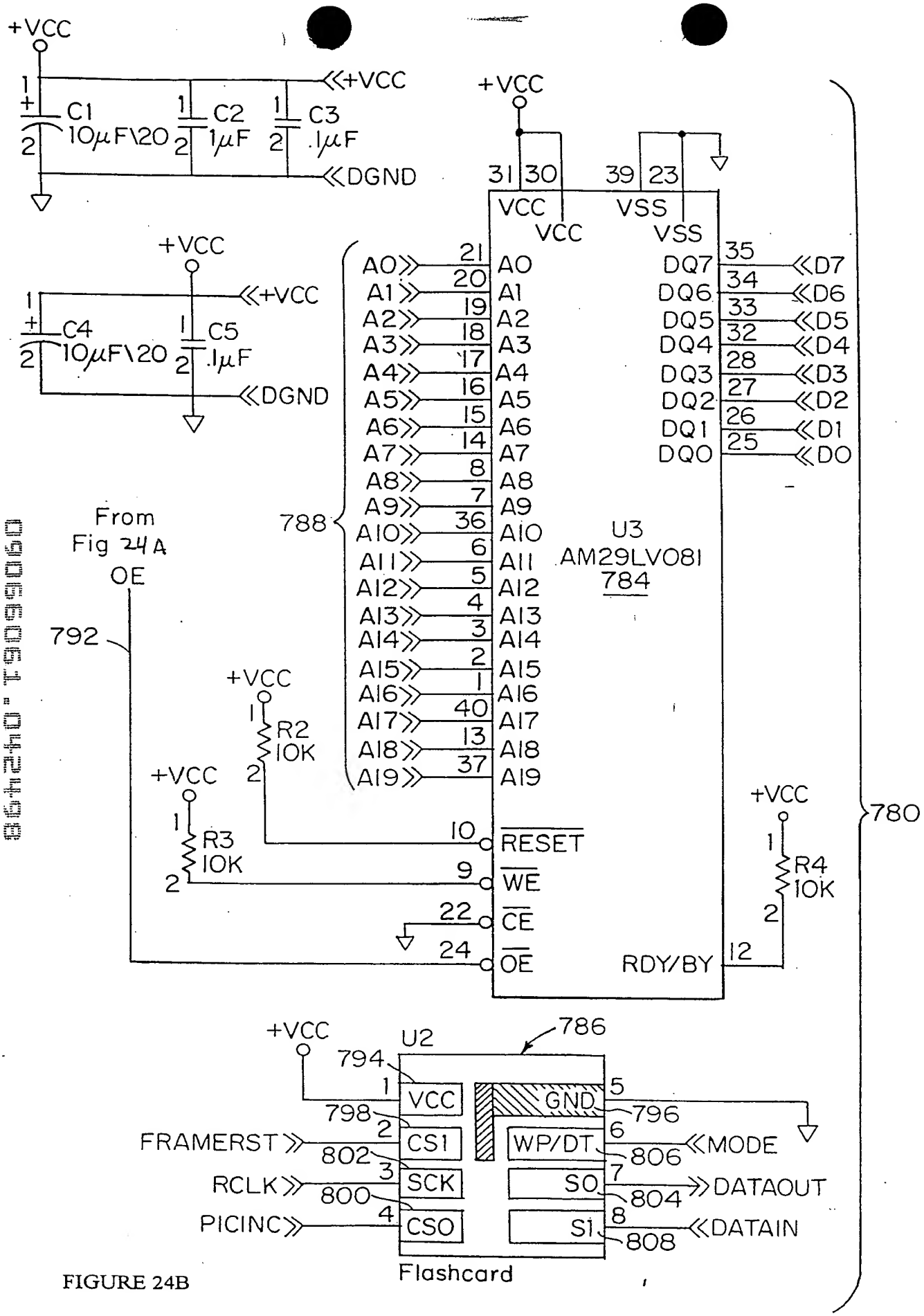

+VCC
C1
10μF\20
C2
1μF
C3
.1μF
DGND
C4
10μF\20
C5
.1μF
VCC
VSS
U3
AM29LV081
784
788
780
From
Fig 24A
OE
792
R2
10K
R3
10K
R4
10K
RESET
WE
CE
OE
RDY/BY
U2
786
794
798
802
800
GND
796
WP/DT
806
SO
804
SI
808
FRAMERST
RCLK
PICINC
MODE
DATAOUT
DATAIN
Flashcard

FIGURE 24B

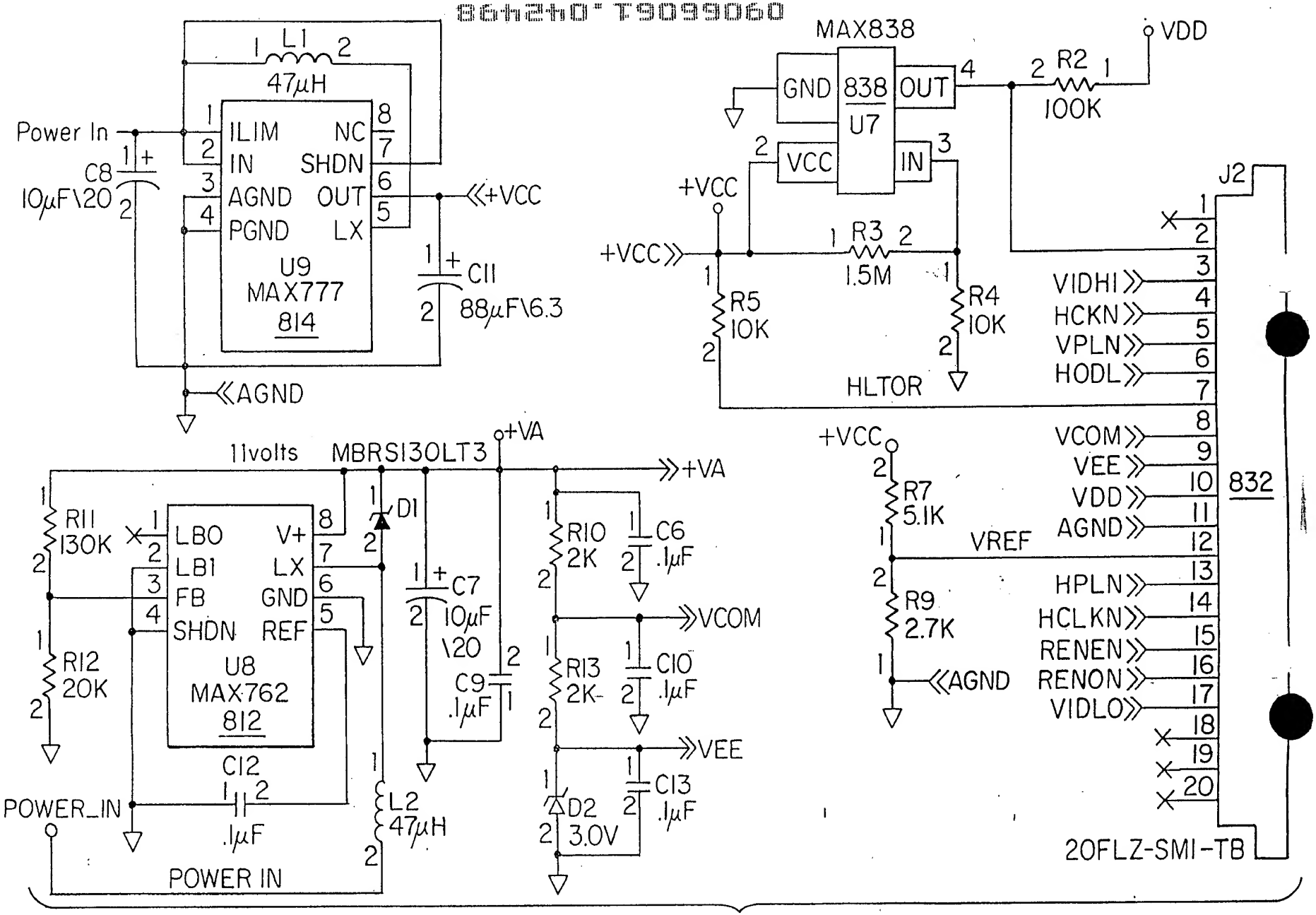


FIGURE 25A

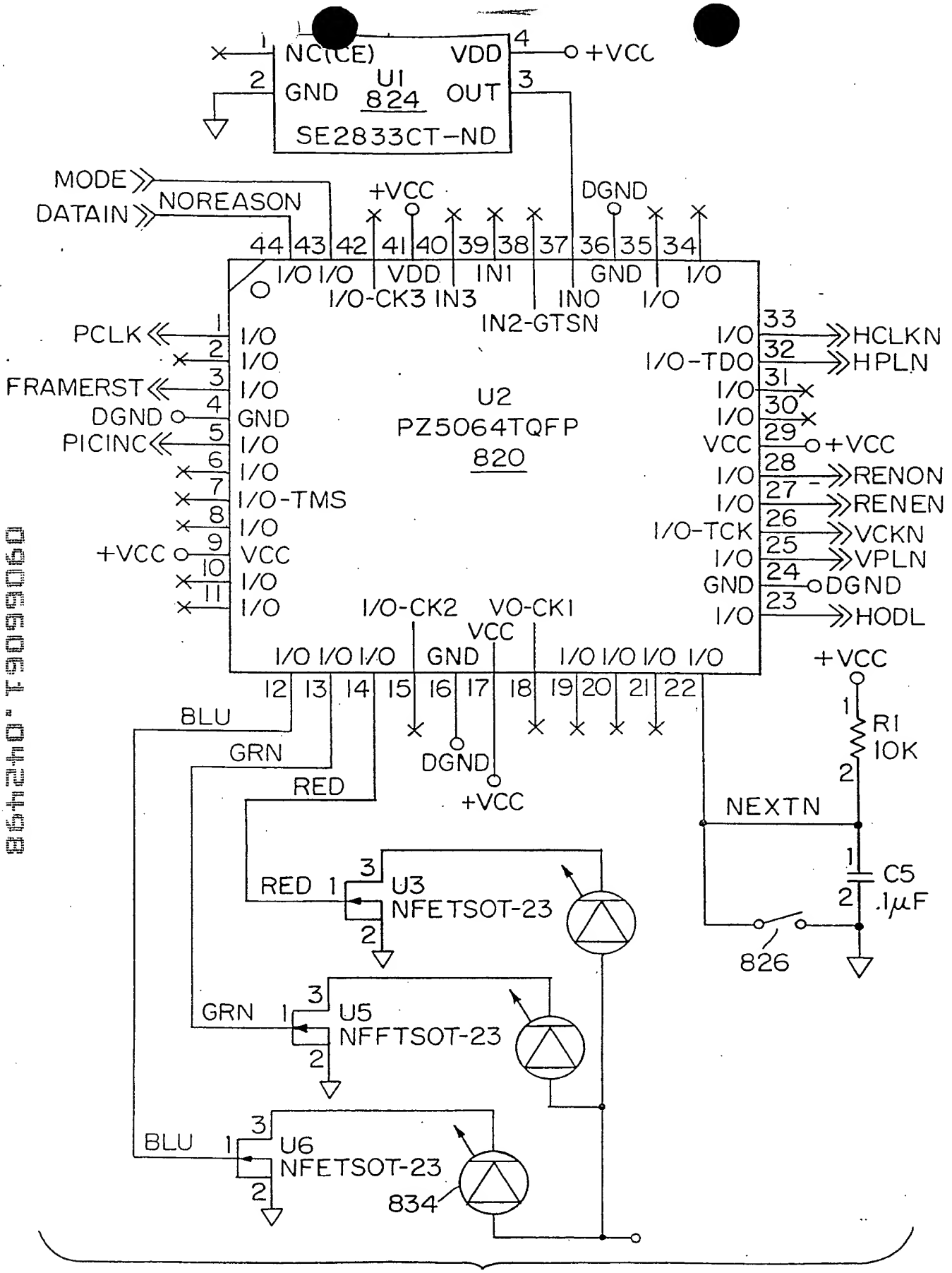

U1
824
SE2833CT-ND
NC(CE)
VDD
GND
OUT
+VCC
MODE
DATAIN
NOREASON
DGND
U2
PZ5064TQFP
820
PCLK
FRAMERST
PICINC
I/O-TMS
I/O-TCK
I/O-TDO
IN2-GTSN
HCLKN
HPLN
RENON
RENEN
VCKN
VPLN
HODL
BLU
GRN
RED
R1
10K
NEXTN
C5
.1μF
826
U3
NFETSOT-23
U5
NFFTSOT-23
U6
NFETSOT-23
834

FIGURE 25B

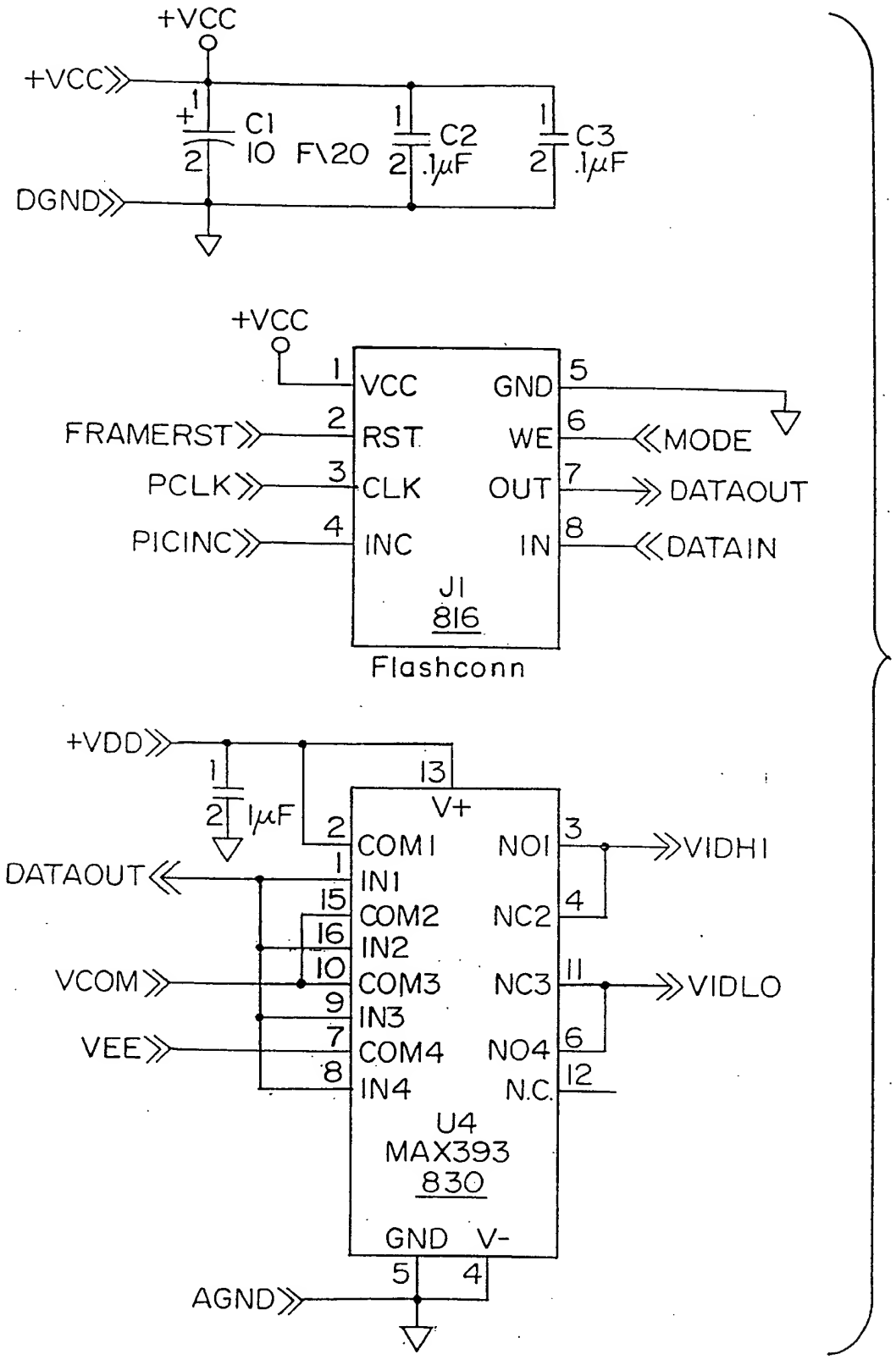

+VCC
+VCC
C1
10 F\20
C2
.1μF
C3
.1μF
DGND
+VCC
VCC
GND
FRAMERST
RST
WE
MODE
PCLK
CLK
OUT
DATAOUT
PICINC
INC
IN
DATAIN
J1
816
Flashconn
+VDD
1μF
V+
COM1
NO1
VIDHI
DATAOUT
IN1
COM2
NC2
IN2
VCOM
COM3
NC3
VIDLO
IN3
VEE
COM4
NO4
IN4
N.C.
U4
MAX393
830
GND
V-
AGND

FIGURE 25C

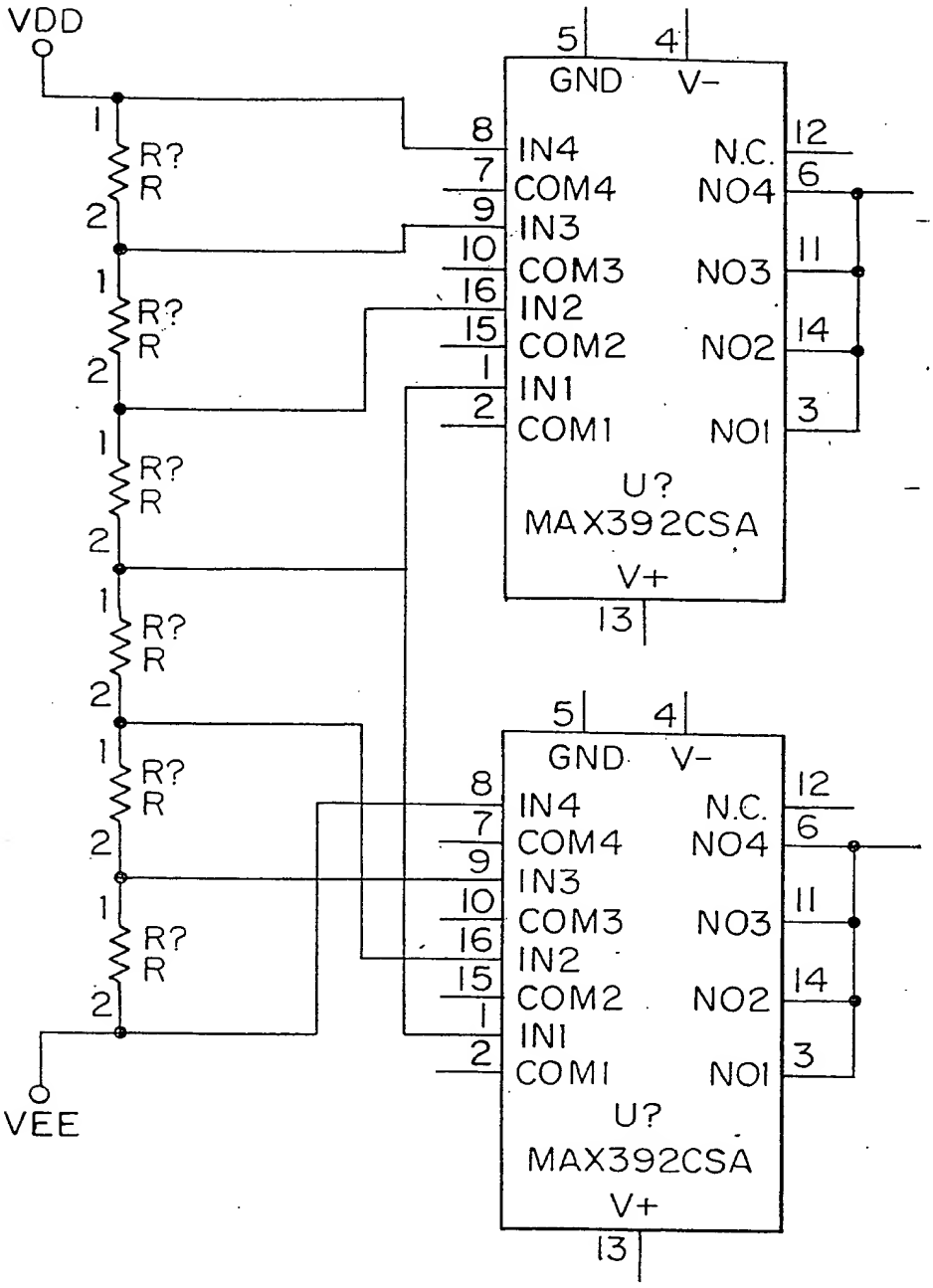

VDD
VEE
R?
R
U?
MAX392CSA
GND
V-
V+
IN4
COM4
IN3
COM3
IN2
COM2
IN1
COM1
N.C.
NO4
NO3
NO2
NO1

FIGURE 26

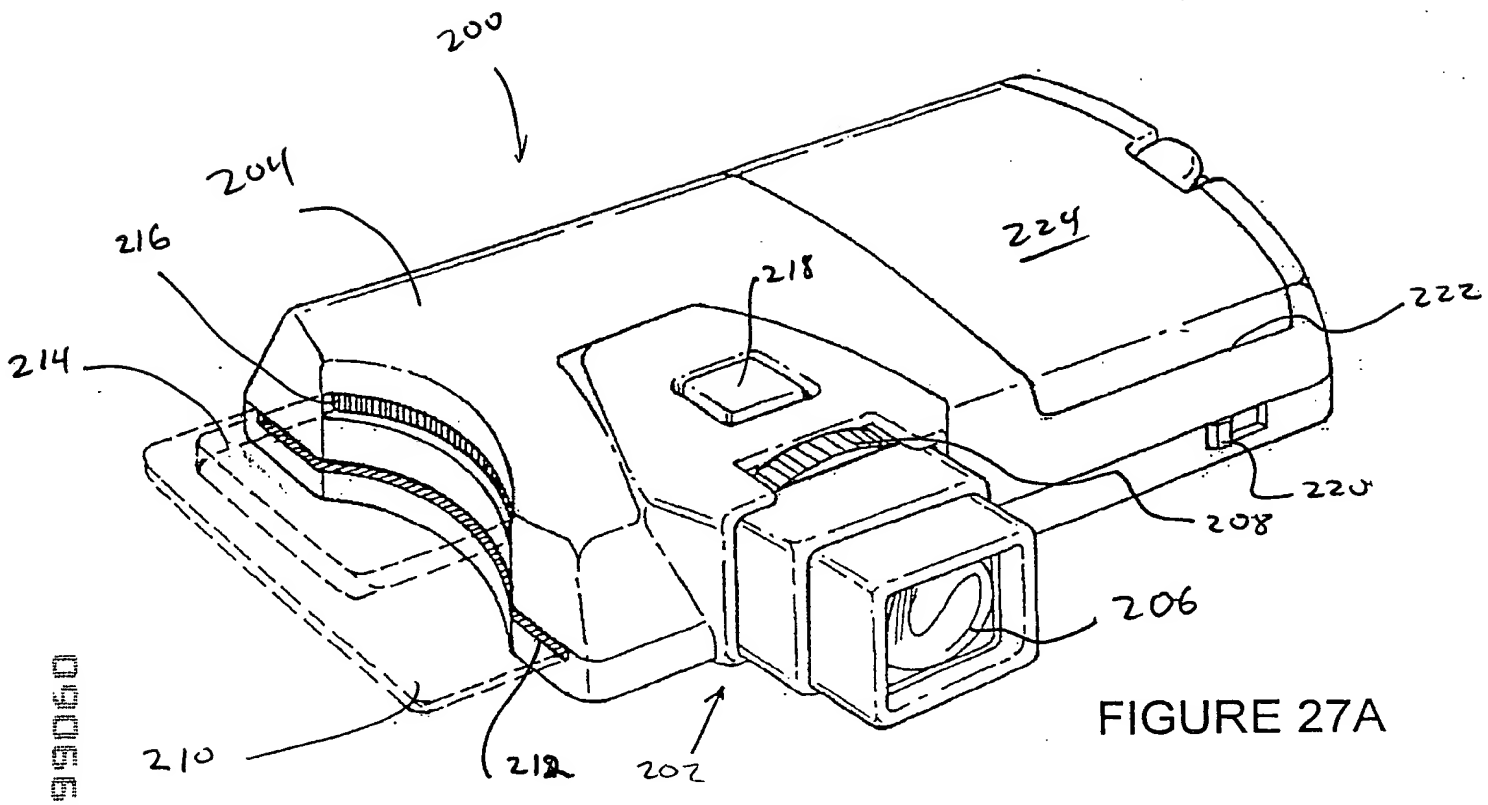


FIGURE 27A

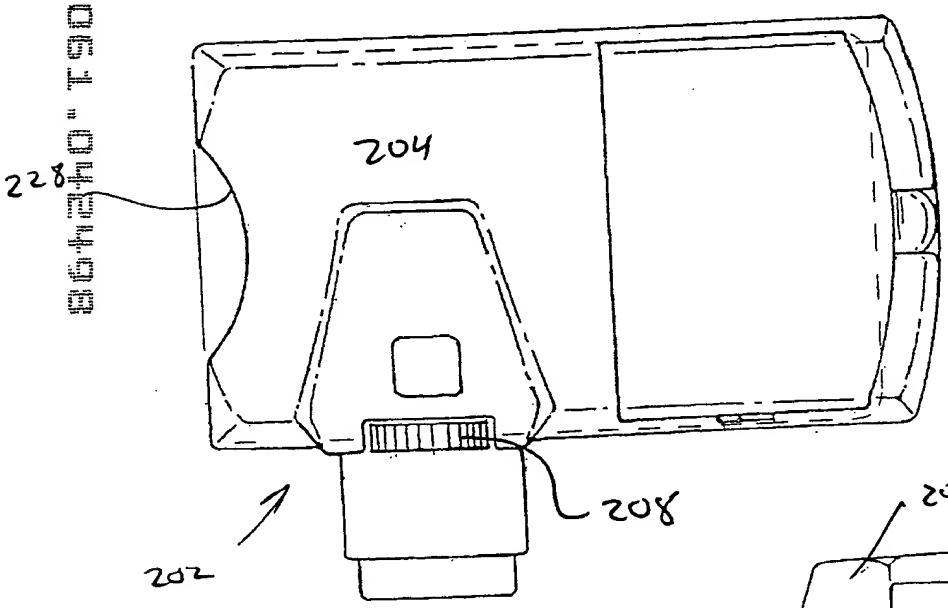


FIGURE 27B

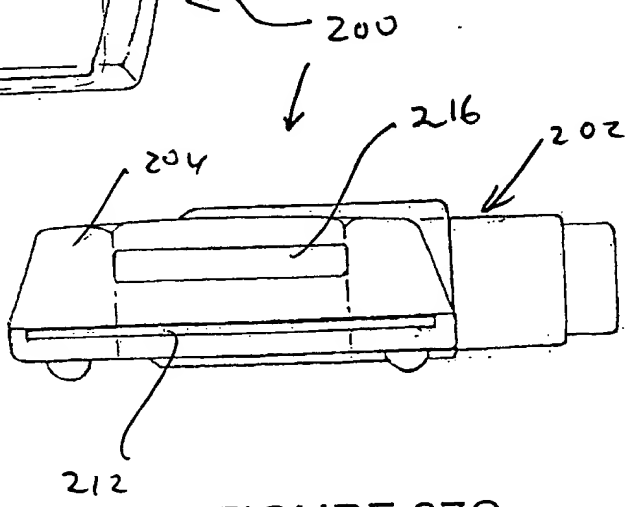


FIGURE 27C

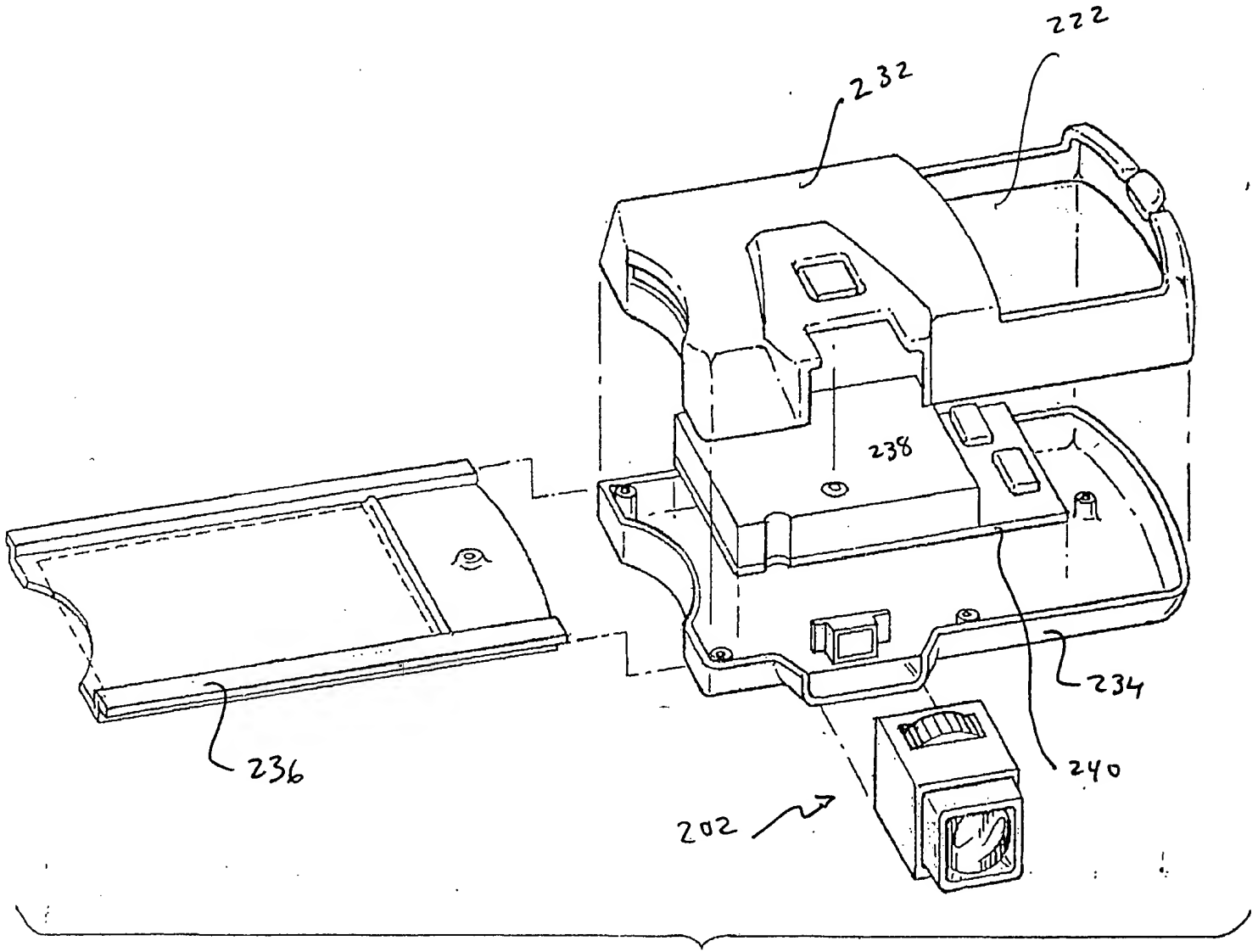


FIGURE 27D

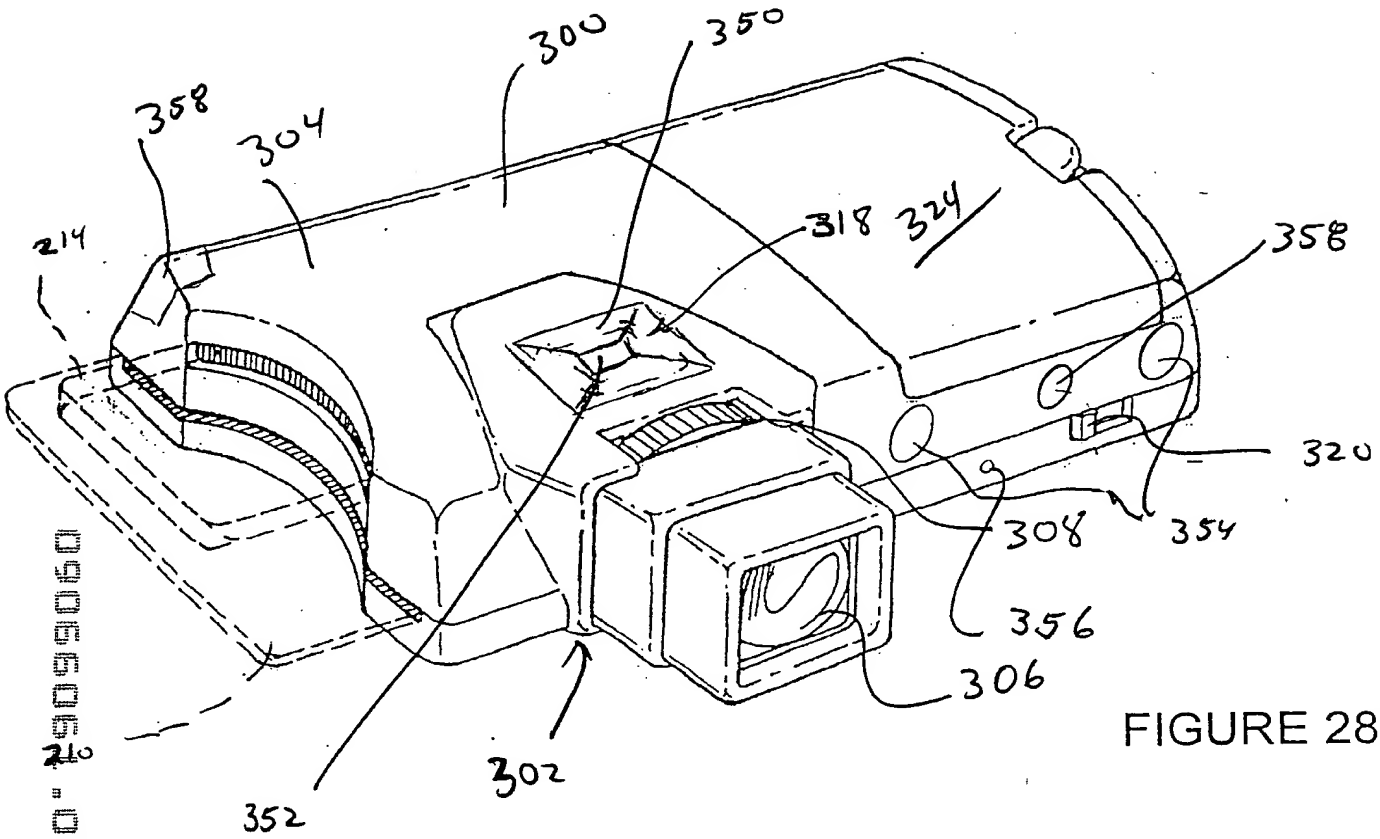


FIGURE 28A

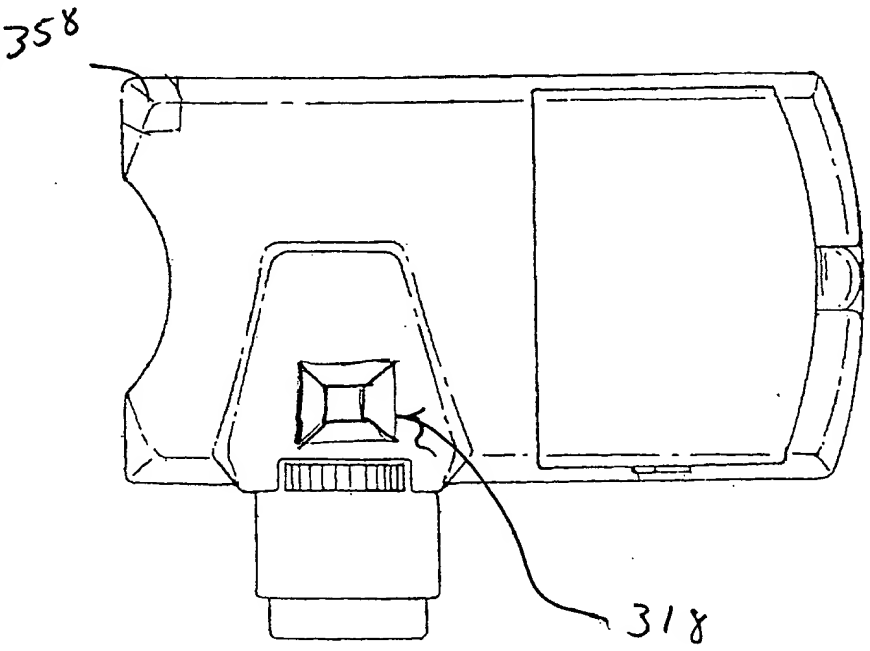


FIGURE 28B

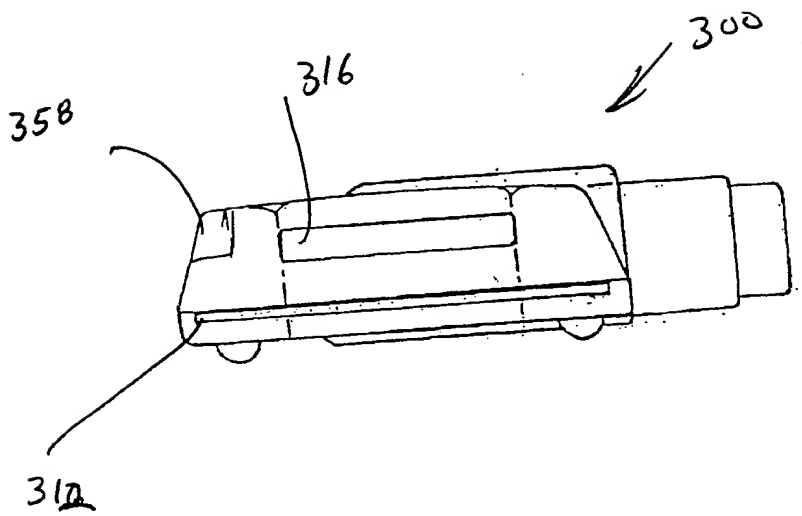


FIGURE 28C

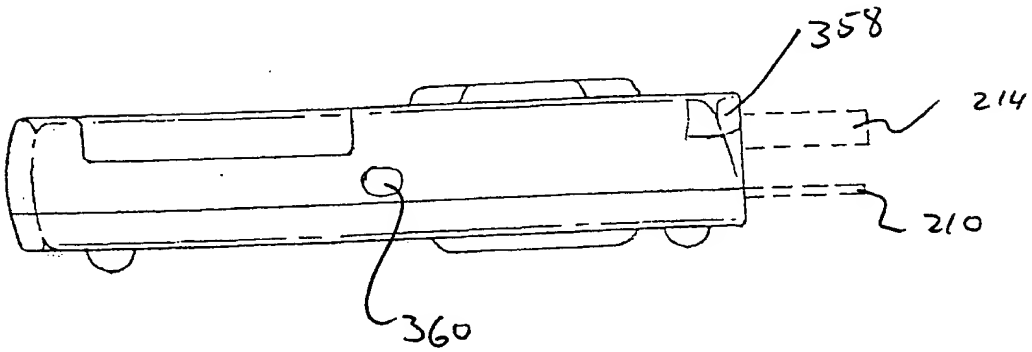
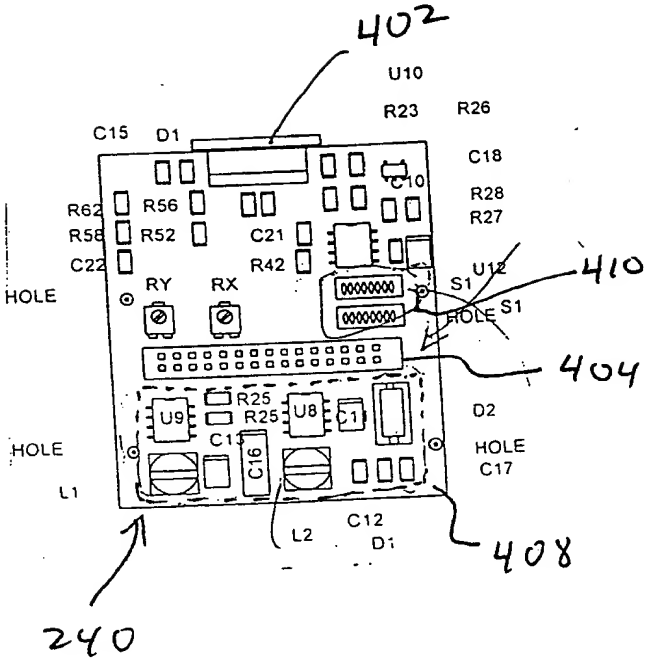


FIGURE 28D

FIGURE 29Aa



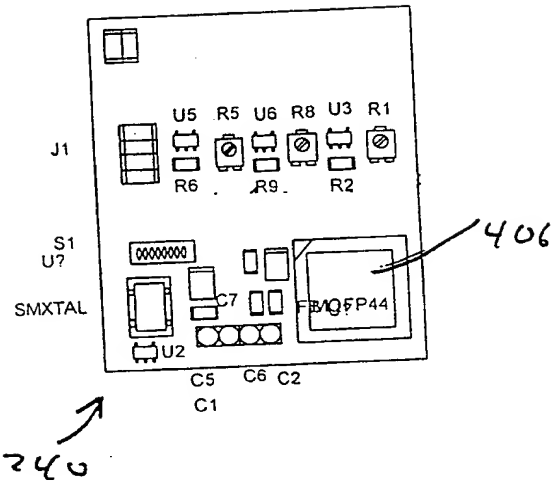


FIGURE 29Ab

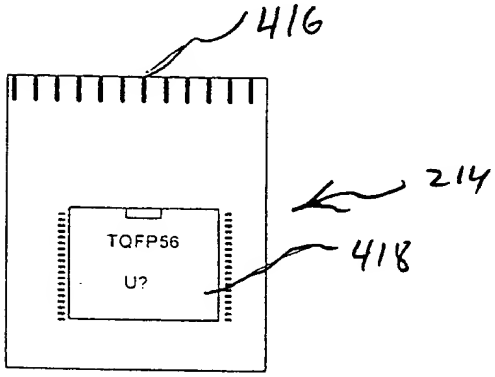


FIGURE 29Ba

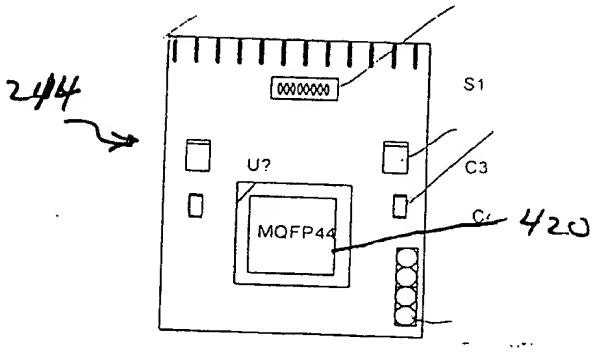


FIGURE 29Bb

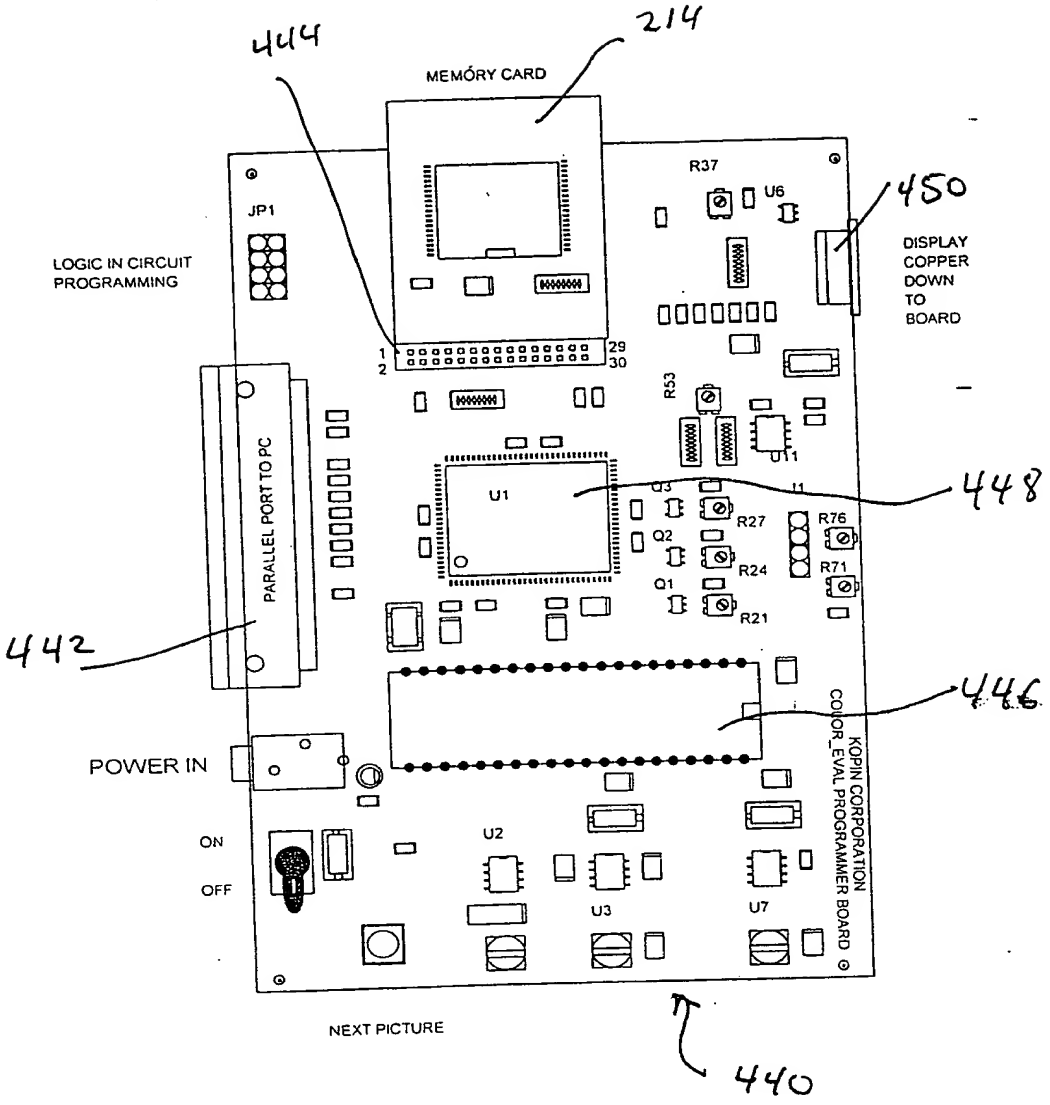

444
214
MEMORY CARD
450
DISPLAY COPPER DOWN TO BOARD
LOGIC IN CIRCUIT PROGRAMMING
JP1
R37
U6
1
2
29
30
R53
U1
448
Q3
R27
R76
Q2
R24
R71
Q1
R21
442
PARALLEL PORT TO PC
446
POWER IN
ON
OFF
U2
U3
U7
KOPIN CORPORATION
COLOR_EVAL PROGRAMMER BOARD
NEXT PICTURE
440

FIGURE 29C

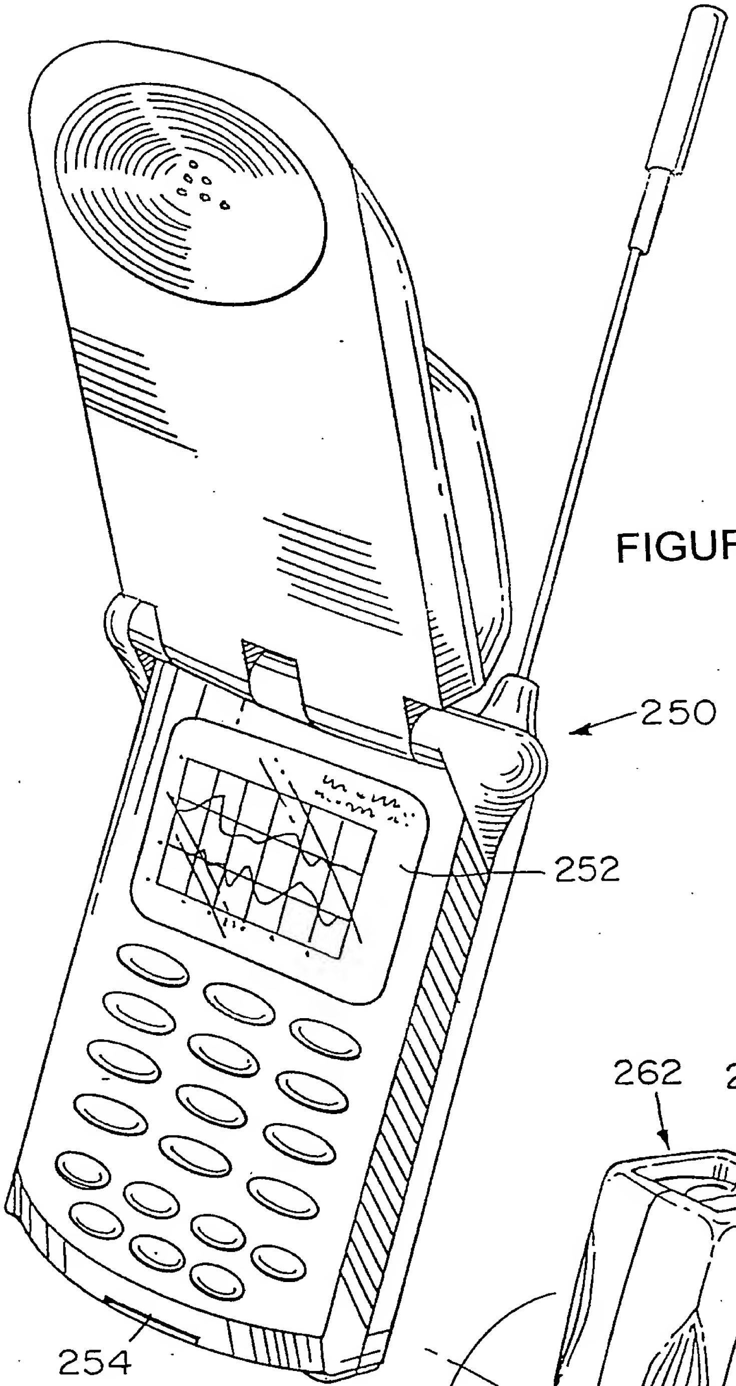


FIGURE 30A

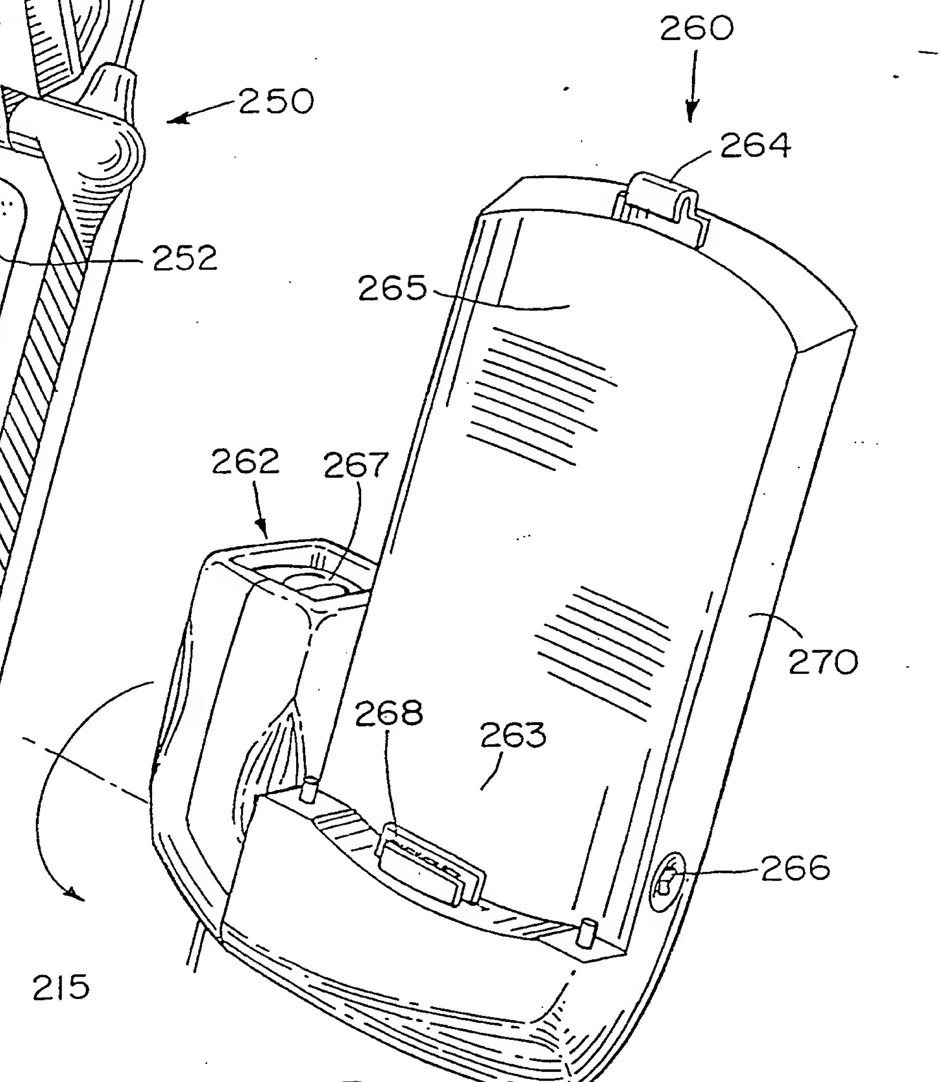


FIGURE 30B

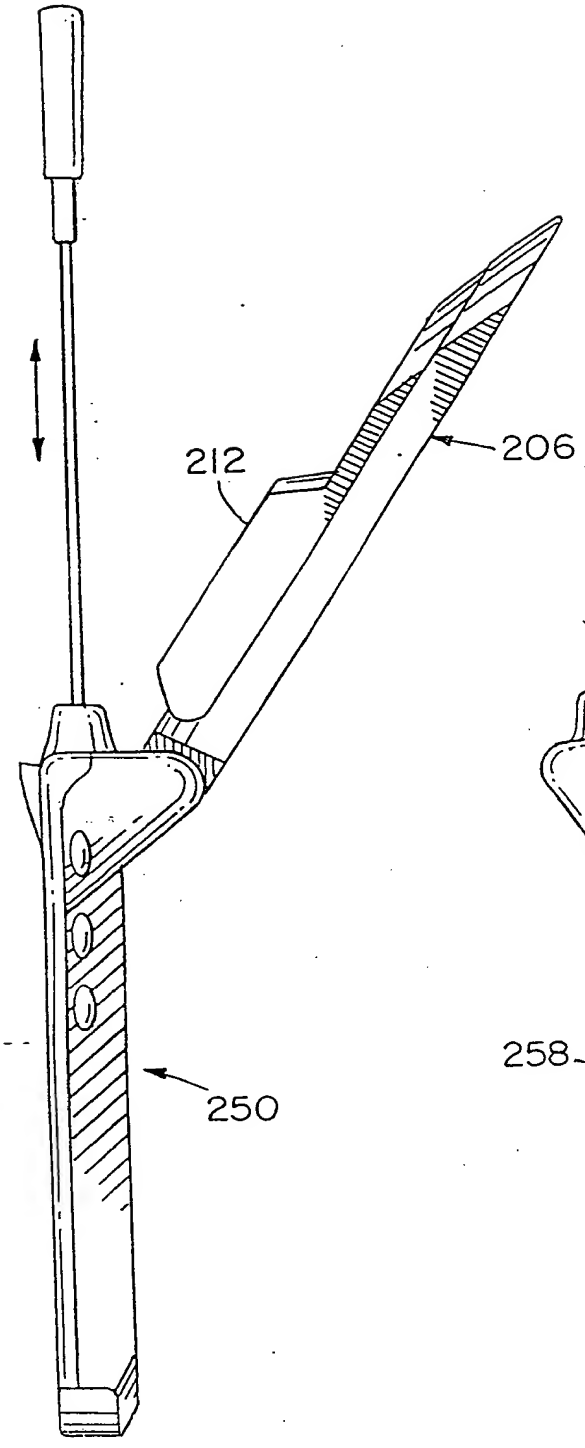


FIGURE 30C

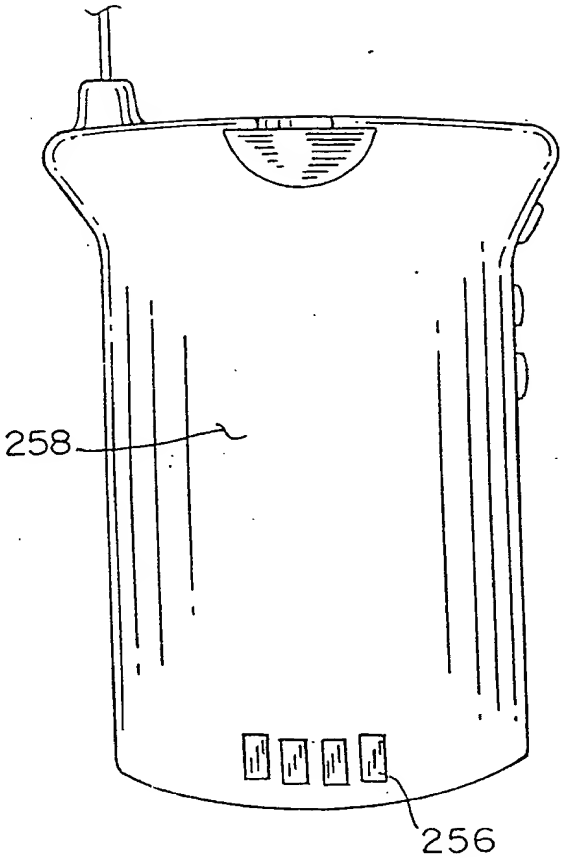


FIGURE 30D

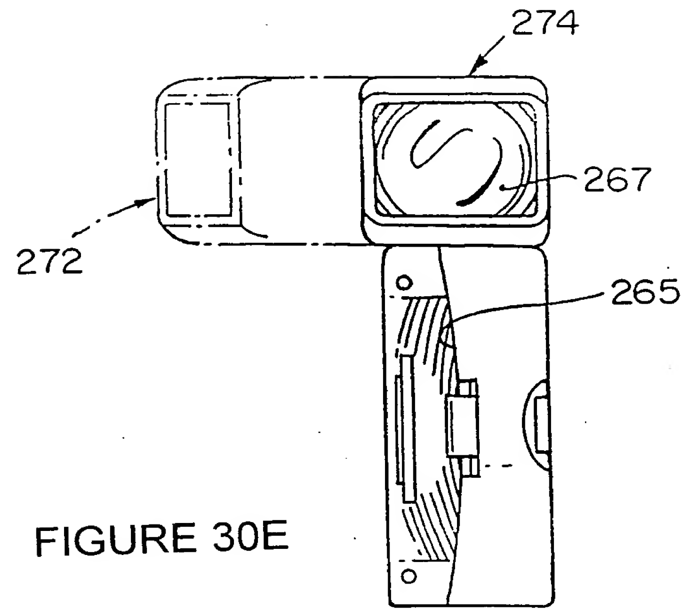


FIGURE 30E

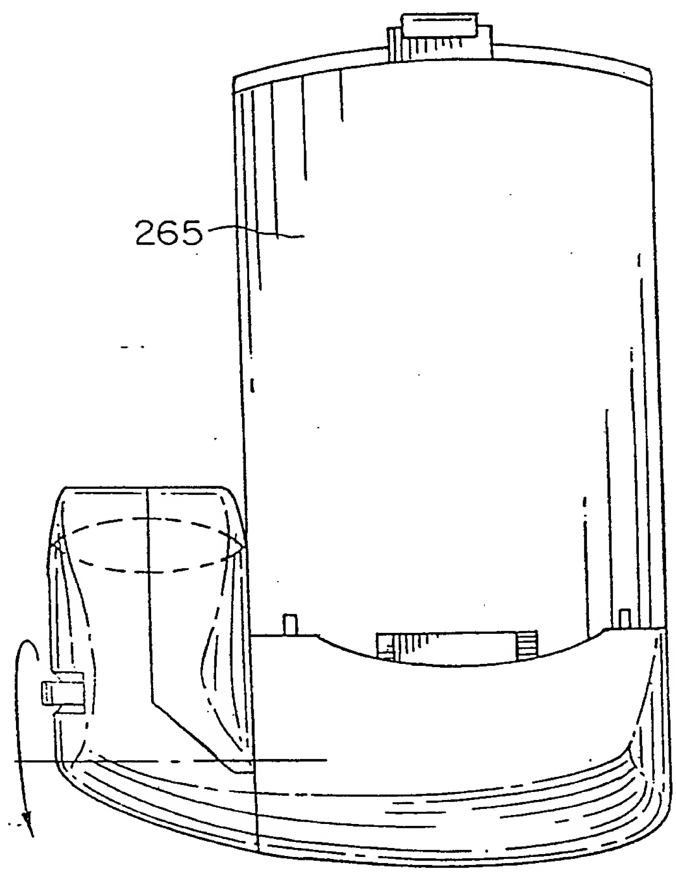


FIGURE 30F

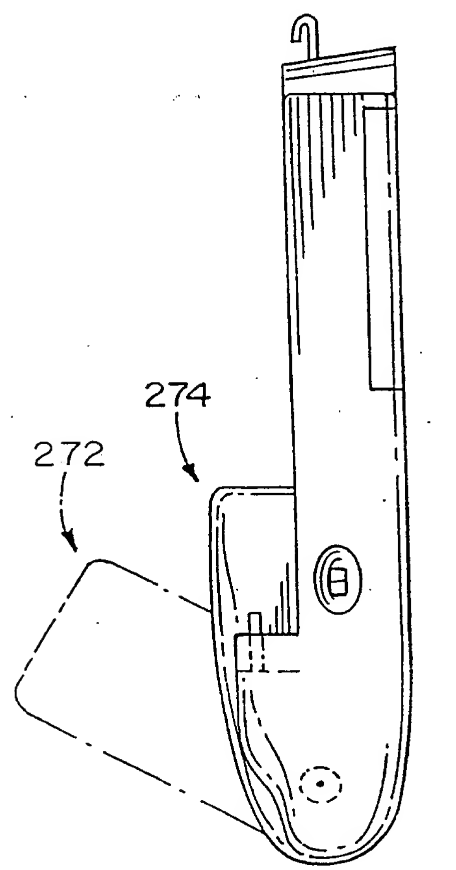


FIGURE 30G

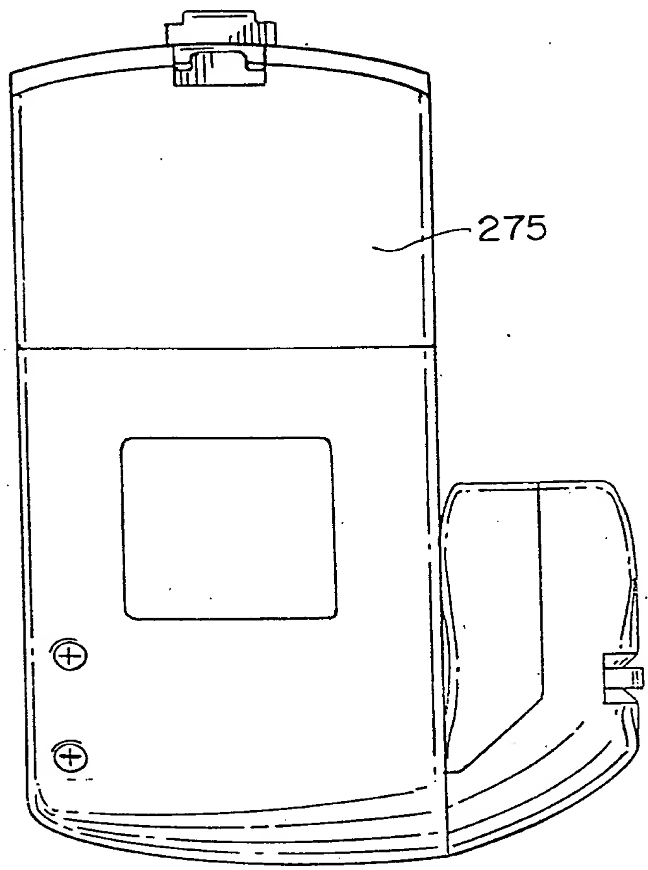


FIGURE 30H

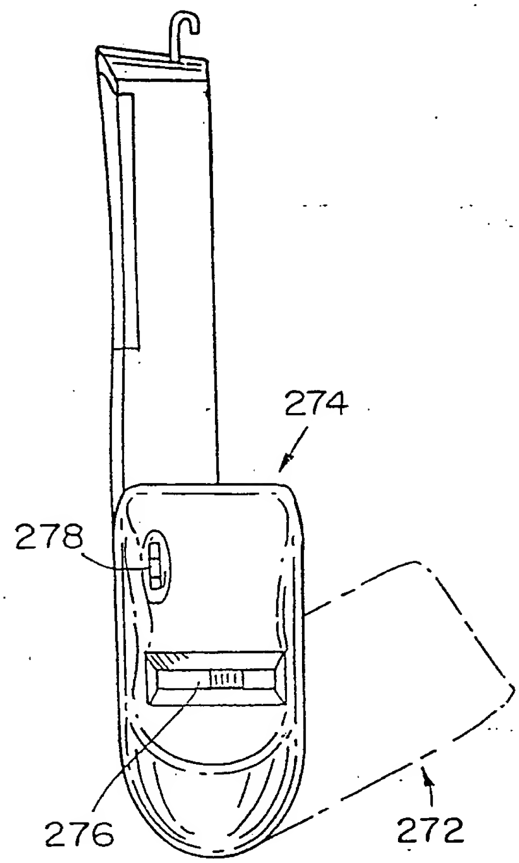


FIGURE 30I

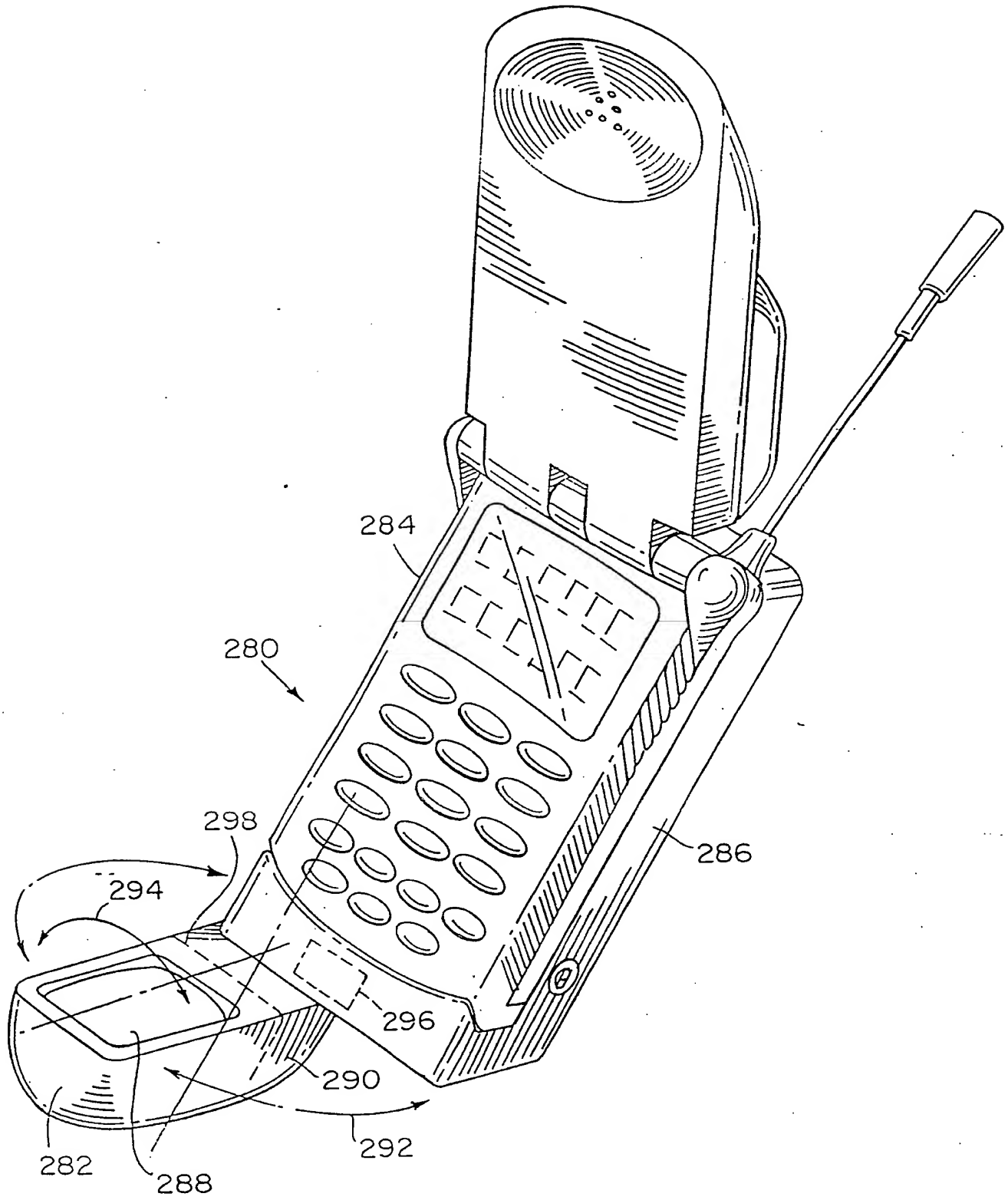


FIGURE 30J

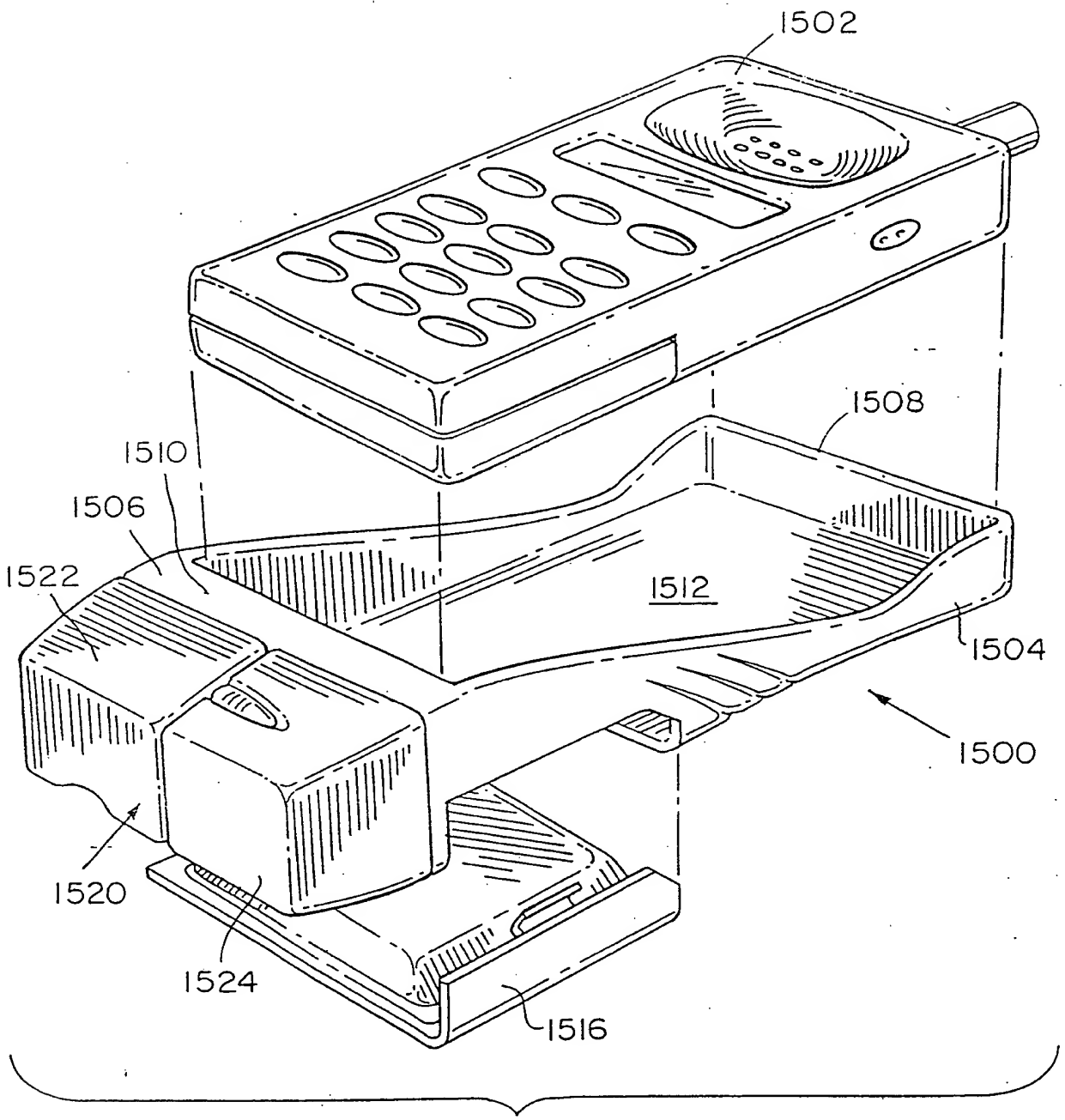


FIGURE 31A

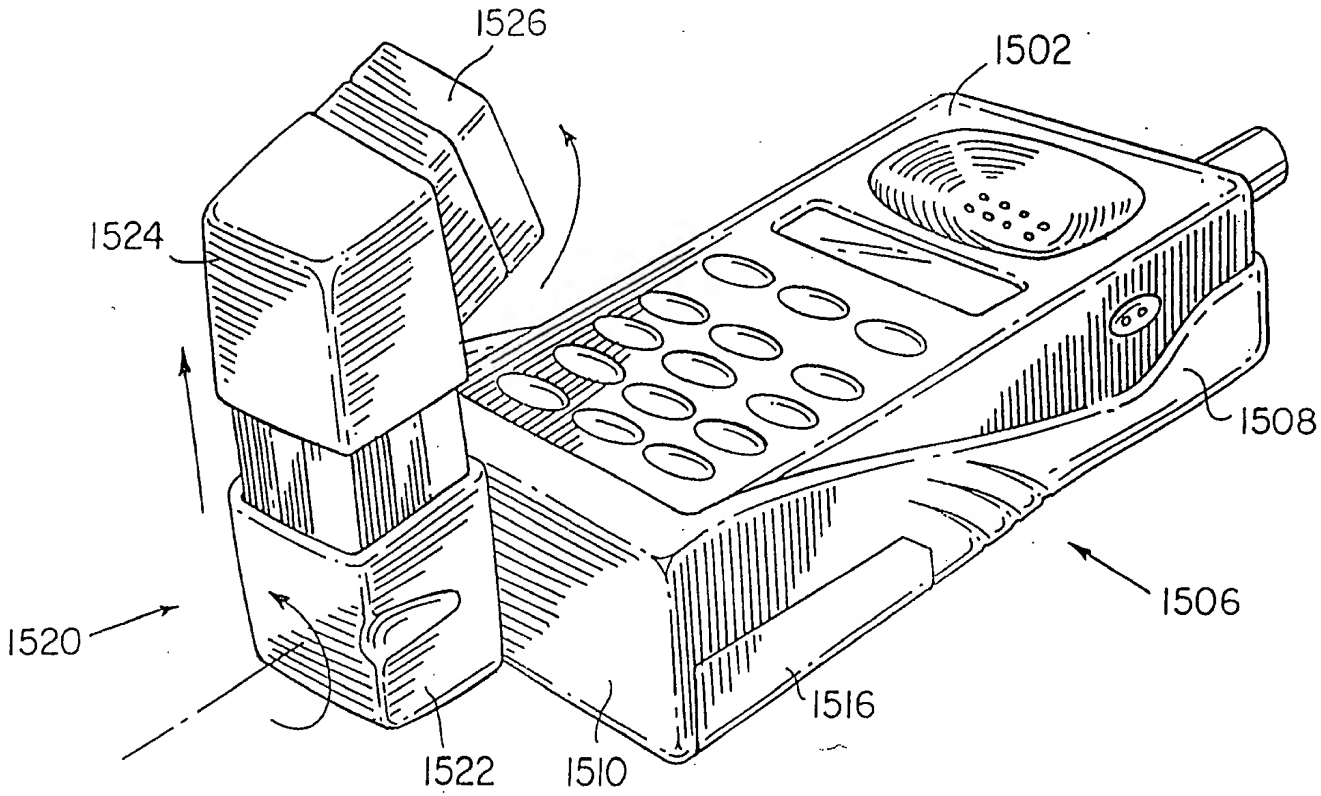


FIGURE 31B

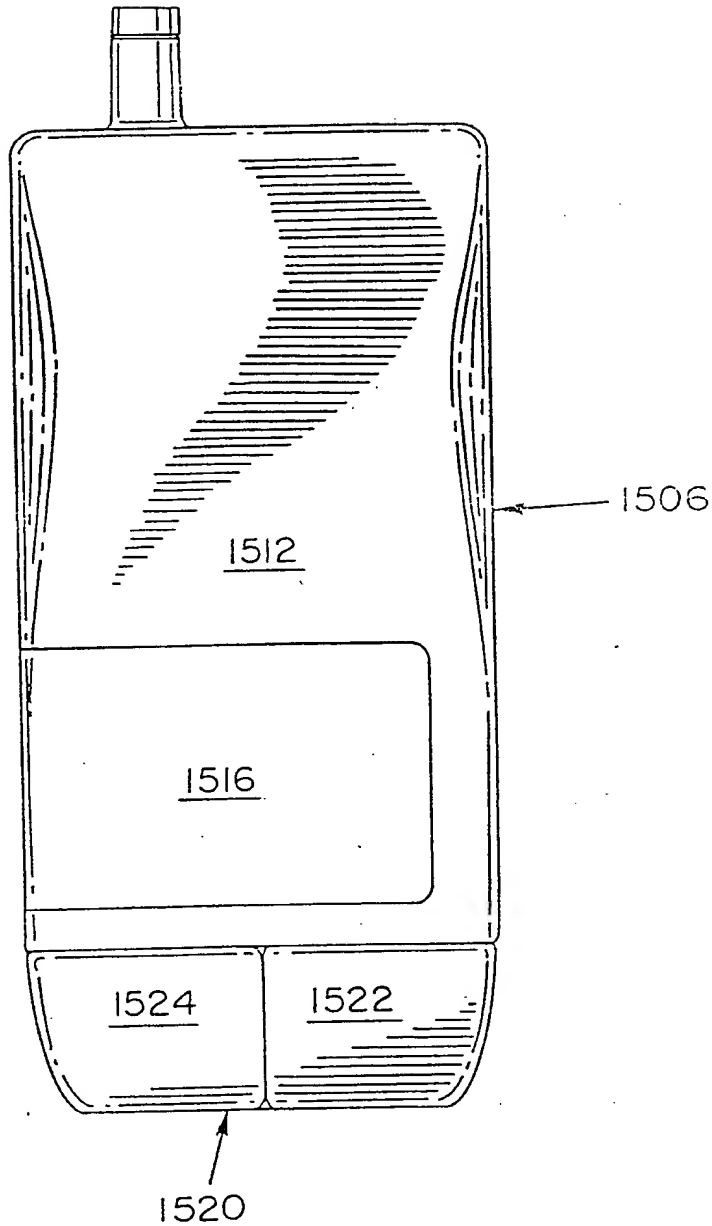


FIGURE 31C

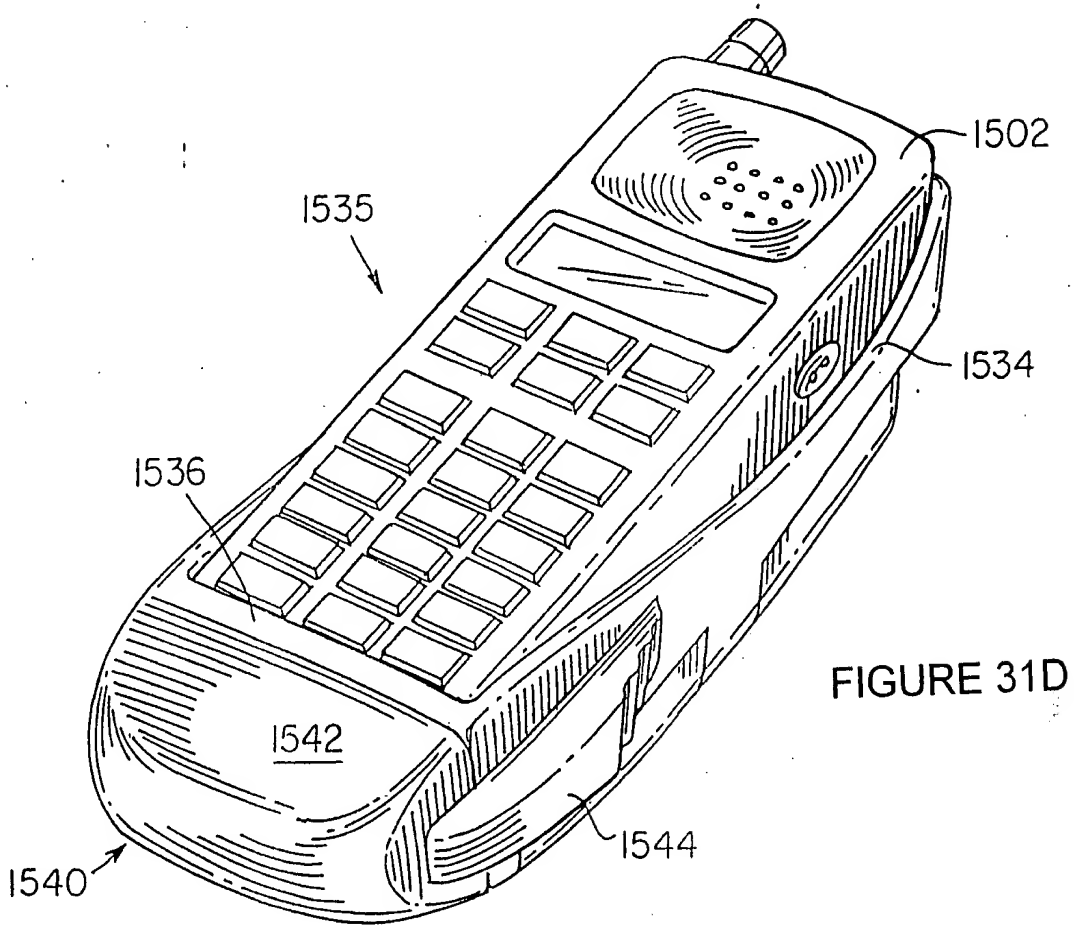


FIGURE 31D

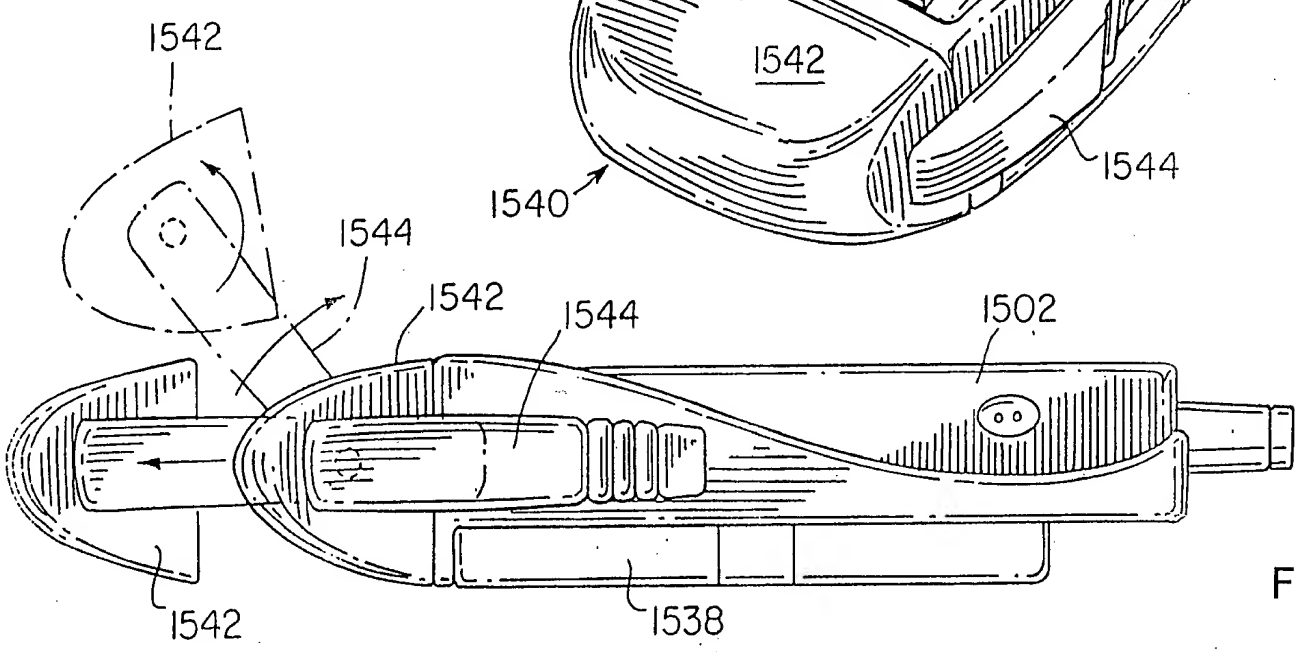


FIGURE 31E

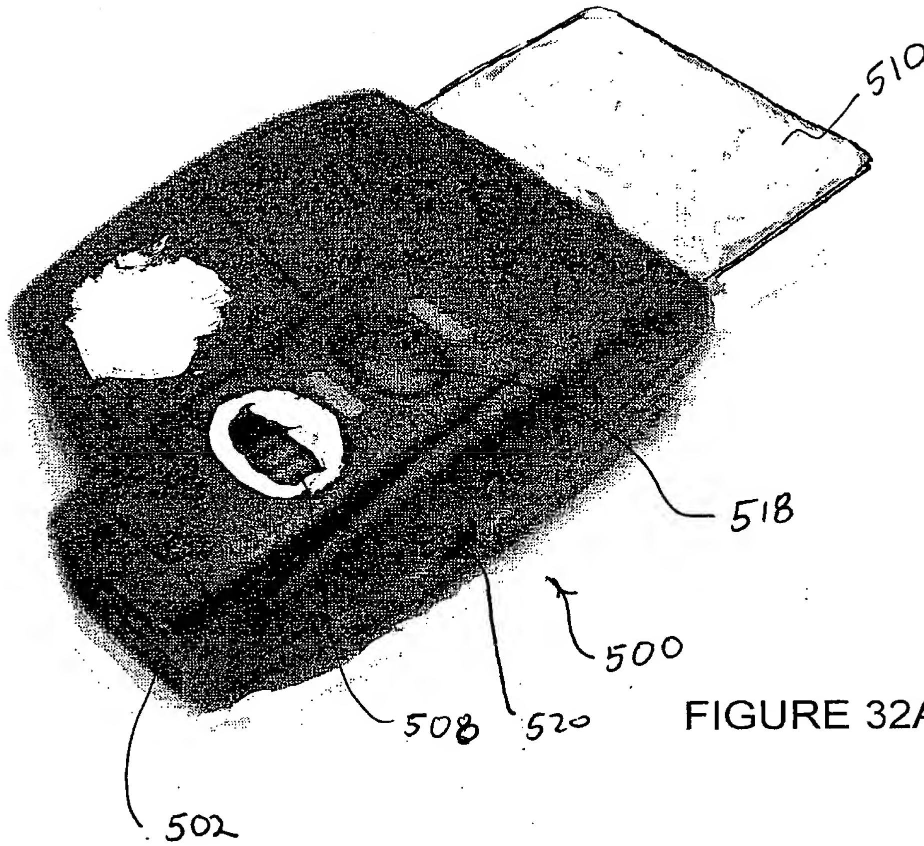


FIGURE 32A

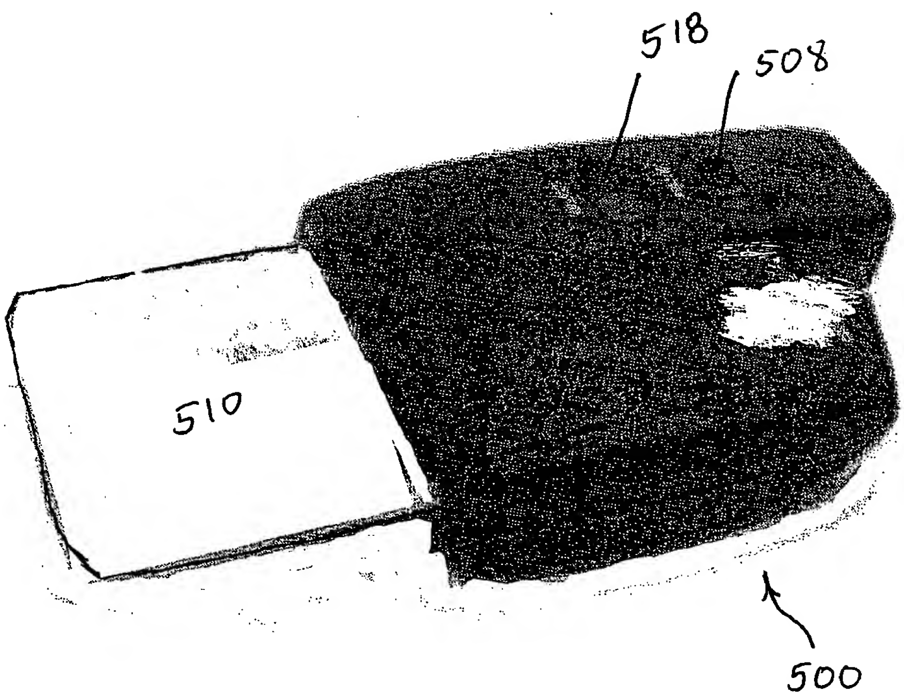


FIGURE 32B

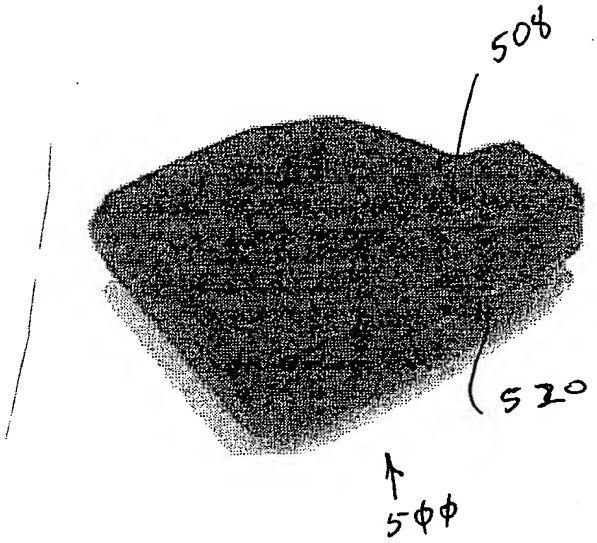


FIGURE 32C

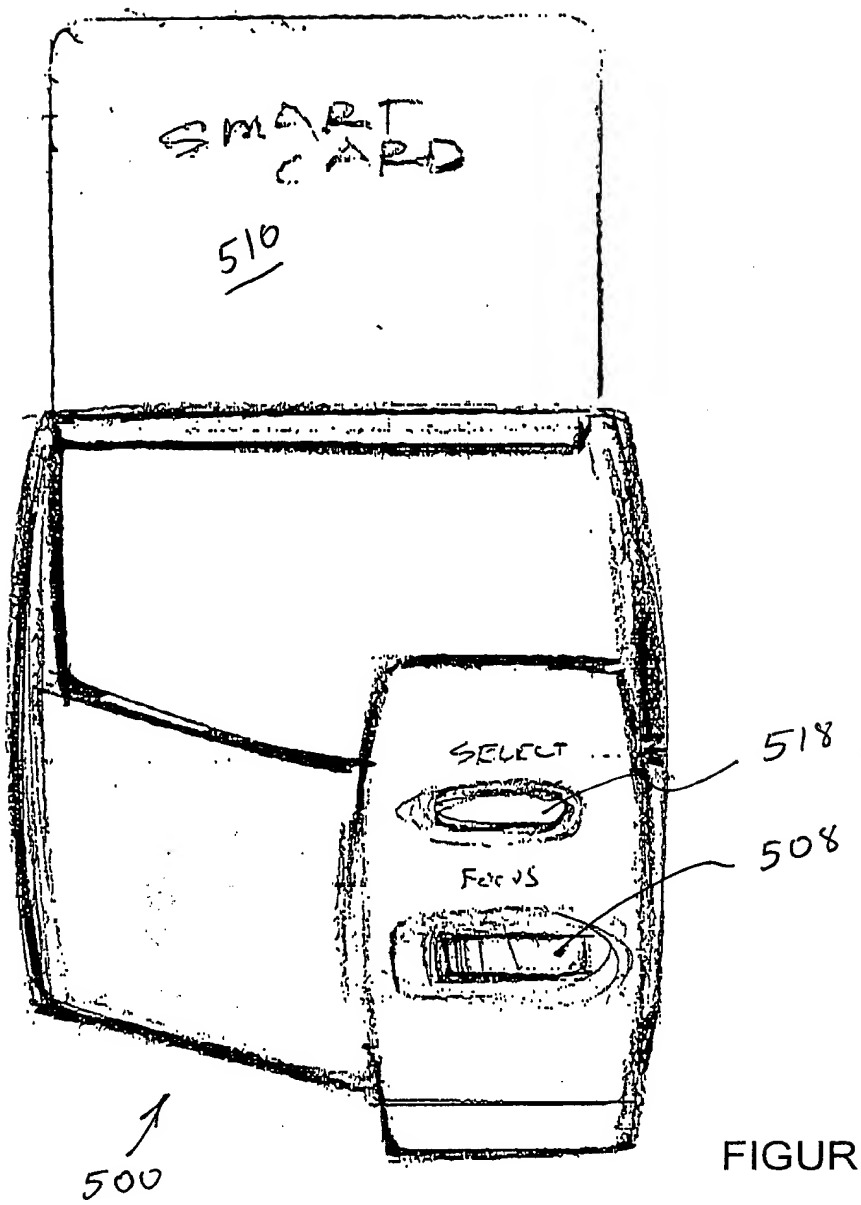


FIGURE 32D

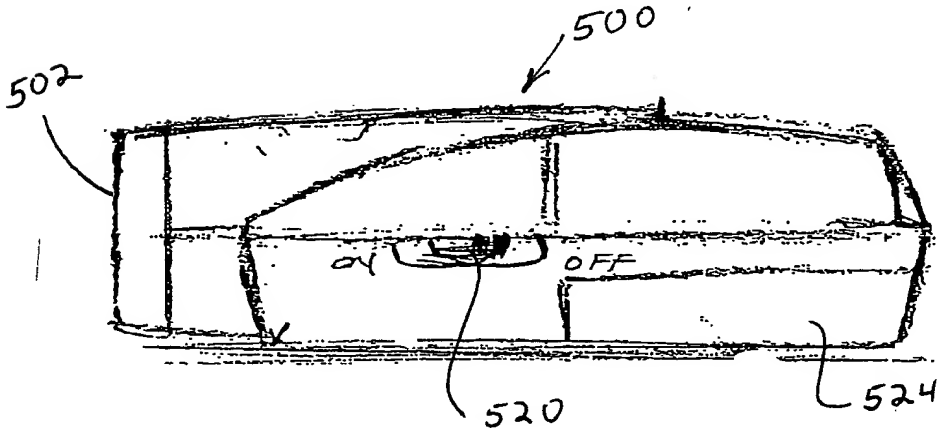


FIGURE 32E

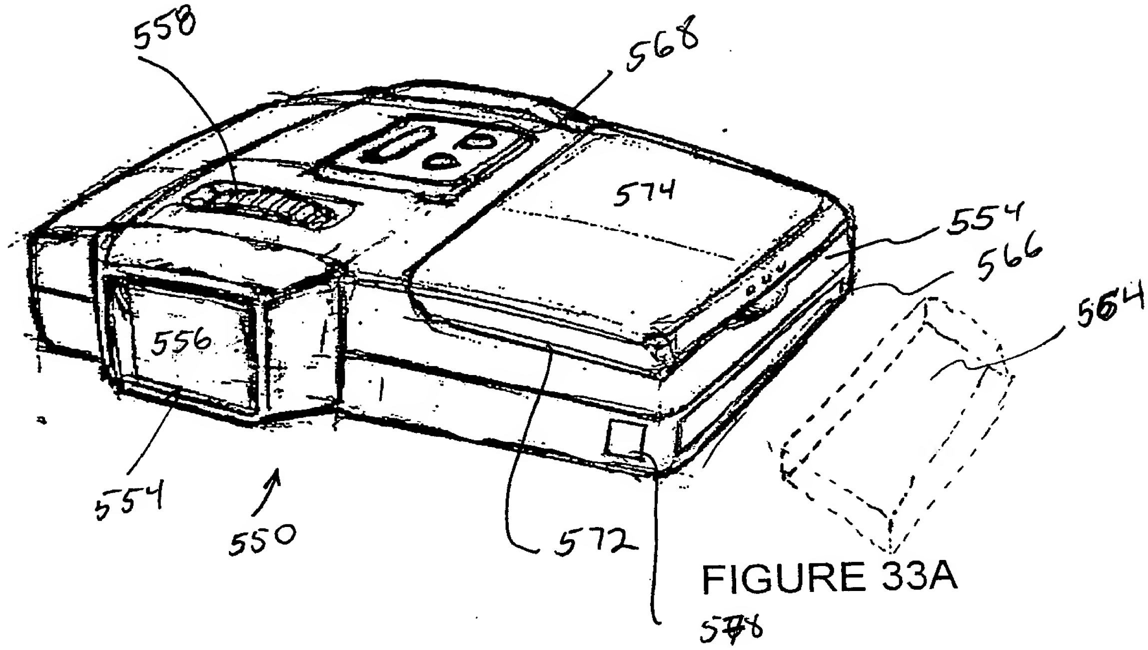


FIGURE 33A

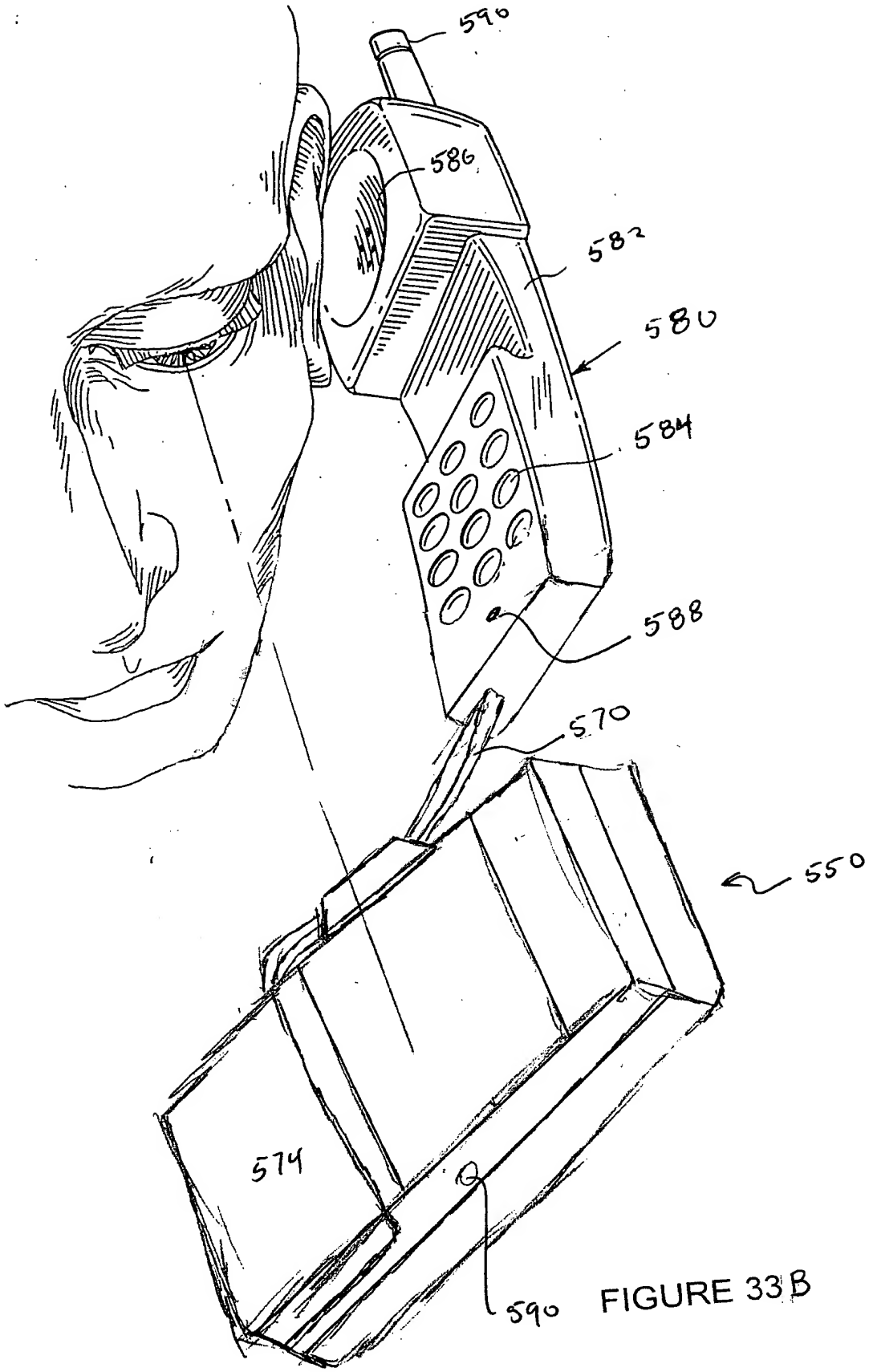


FIGURE 33B

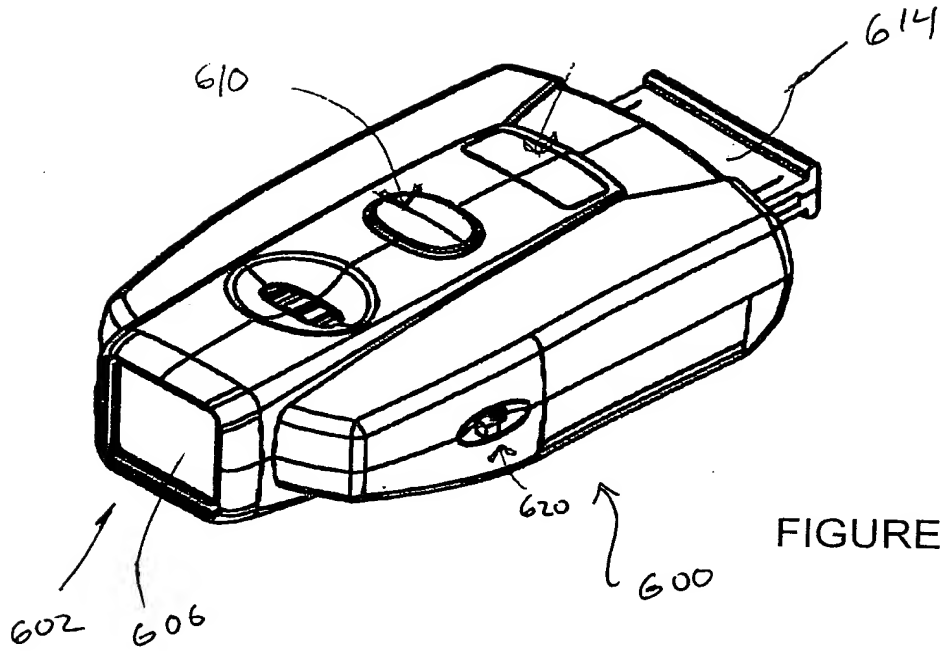


FIGURE 34A

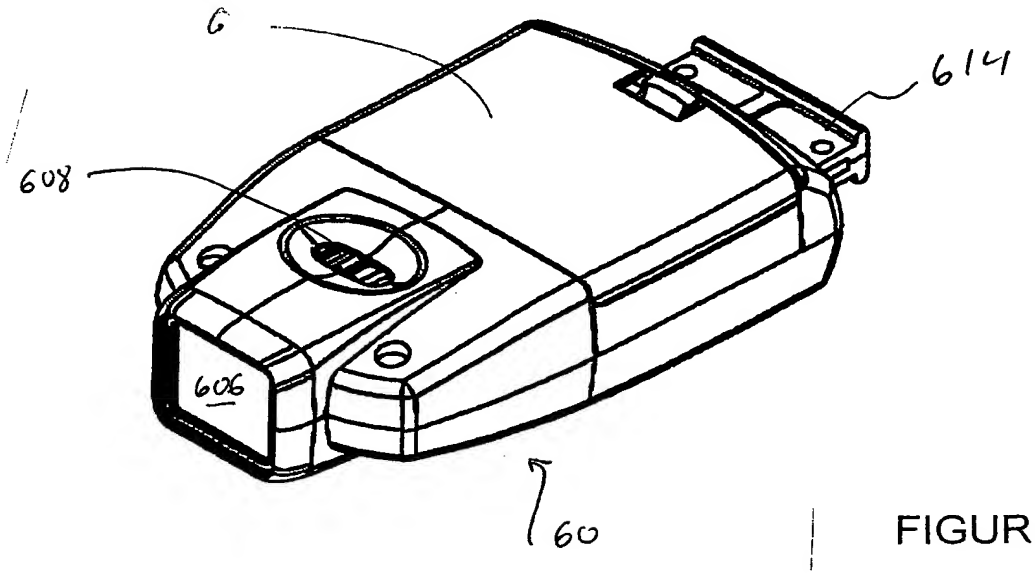


FIGURE 34B

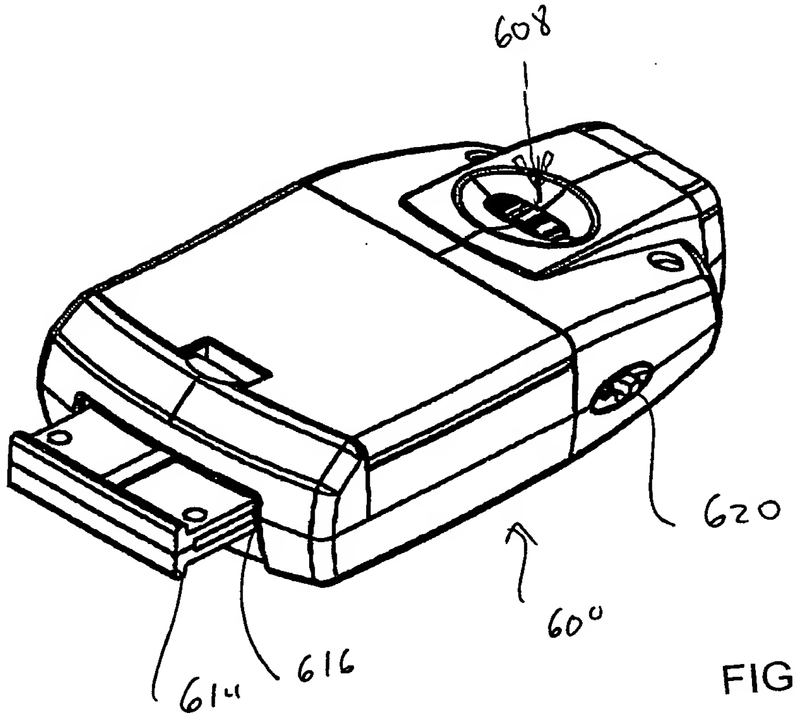


FIGURE 34C

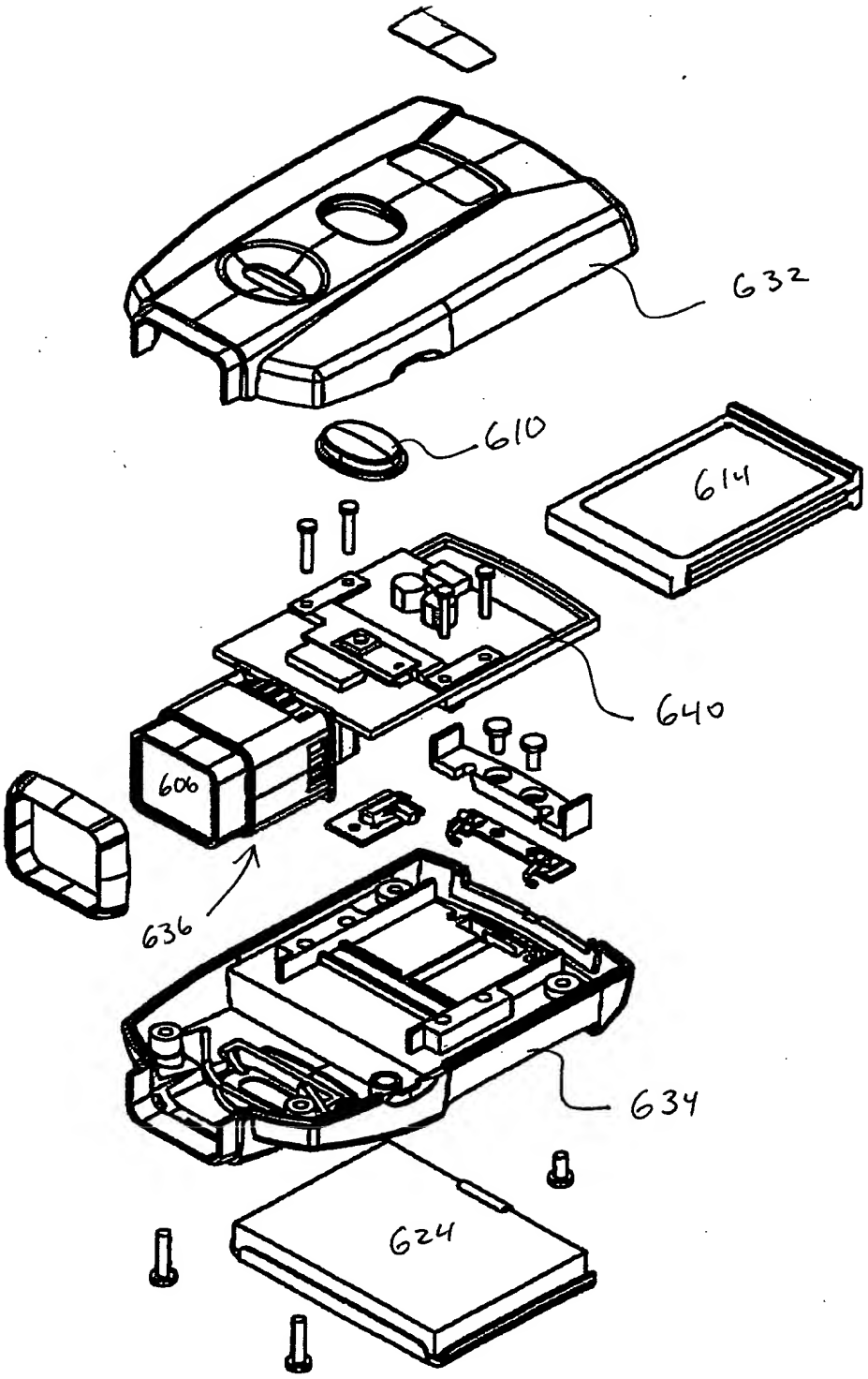


FIGURE 34D